BE-T1000 (Baikal-T1) Microprocessor

Datasheet

Document ID: BE-T1-DS-Eng#928

1 Introduction

The BE-T1000 (formerly known as Baikal-T1) is a general purpose *System-on-a-Chip* (**SoC**) designed to use in embedded systems, industrial automation, and communication solutions, which require low power consumption with high performance and wide I/O features. It can also be used in computing systems, such as zero and thin clients, POS devices, and HMI devices.

The SoC includes a dual-core MIPS32® P5600™ series processor system, which operates at 1.2 GHz and supports extended command binding featured in the latest generations of Imagination MIPS®.

The BE-T1000 contains a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 2.0, SATA 6G, I^2C, SPI, UART, and GPIO.

It consumes less than 5W of power.

1.1 Main Features

Table 1-1 The SoC Main features

Feature	Description
Dual-Core Cluster Subsystem	MIPS32 architecture
	Two P-Class P5600 r5 cores operating at 1.2 GHz
	128 KB Level 1 cache (64 KB data cache + 64 KB instruction cache) in a core
	1 MB Level 2 cache controlled by Coherence Manager
	MIPS Floating Point Unit Gen3 with SIMD
	MIPS *Global Interrupt Controller* (**GIC**) (128 interrupts)
	Embedded Debug Module (EJTAG debug 5.0 port + MIPS PDtrace™)
Main Interconnect	AMBA 3 AXI protocol
	5 AXI channels
	40-bit address width
External memory interface	DDR3-1600 interface
	32-bit SDRAM data width + *Error-correcting code* (**ECC**) width
	40-bit application address width
	Up to 8 GB off-chip SDRAM
High Speed Peripherals	PCIe x4 Gen3 interface
	USB 2.0 controller (ULPI)
	Two SATA 6G interfaces
	10 Gb Ethernet interface (10GBASE-KX4, 10GBASE-KR)
	Two 1 Gb Ethernet controllers (RGMII)
Low Speed Peripherals	Three peripheral timers
	Two GPIO: x3 and x32
	Two UARTs
	Two SPI controllers
	Three I^2C controllers
System Monitoring	PVT controller
	Watchdog timer
Package	HFCBGA-576, 25x25 mm, 1 mm pitch
Power consumption	5W max
Operational temperature	From 0 to +70°C*
Technology	CMOS 28 nm

* Computer simulations show that the SoC is operating at the extended temperature range of -45 to+70°C, but only the standard range of 0 to +70°C has been tested

1.2 Block Diagram

The following figure shows the BE-T1000 SoC functional subsystems.

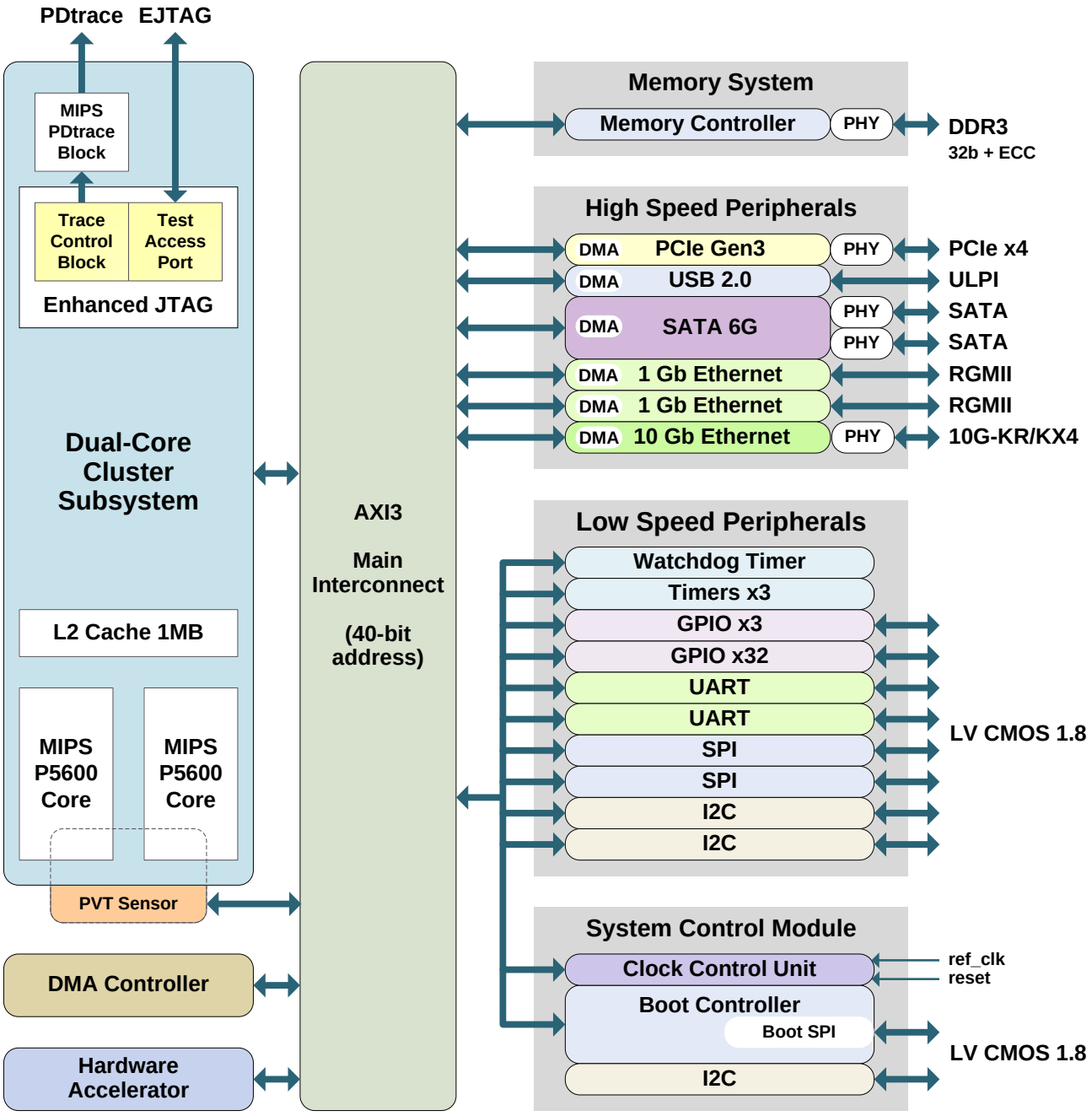

Figure 2-1 BE-T1000 Block Diagram

2 Detailed Description

2.1 Dual-Core Cluster Subsystem

Based on the MIPS32 P5600 Series Multiprocessing System, the subsystem has the following features:

- Two coherent MIPS32 P5600 Series CPU cores operating at 1.2 GHz
- 40-bit address width (*eXtended Physical Addressing* (**XPA**))
- 128 KB Level 1 cache (64 KB data cache + 64 KB instruction cache) in a core
- 1 MB Level 2 cache controlled by Coherence Manager that supports virtualization, XPA, and L2 prefetching
- MIPS Floating Point Unit Gen3 supports scalar FPU and MSA SIMD instructions
- MIPS Global Interrupt Controller handles the distribution of interrupts (up to 128) between and among the cores in the cluster
- Enhanced JTAG block with integrated MIPS PDtrace block provides the following debugging and profiling capabilities:
    - “External” debug—conventional debug through the JTAG interface
    - Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the PDtrace interface to an external debug system

The cluster has integer operations performance per watt higher than most competitors.

2.1.1 Main Interconnect

The Main Interconnect provides interconnection between the SoC modules to create a complete high performance network infrastructure. It is organized as a crossbar switch connecting multiple inputs with multiple outputs.

It complies with AMBA 3 AXI protocol, contains 5 AXI channels and supports 40-bit address width.

2.2 Memory Management

2.2.1 DDR3 Memory Subsystem

The integration of the DDR3 controller and DDR PHY creates a complete solution for connecting the SoC to a DDR memory device of the following type:

- 32-bit DDR3 (speed grades up to DDR3-1600)

The subsystem supports the following features:

- 40-bit application address width (XPA; up to 1 TB DDR memory space)
- 32-bit SDRAM data width
- ECC:
    - *Single error correction/double error detection* (**SEC**/**DED**)
    - 32 data bits + 7 check bits in full bus width mode (16 data bits + 6 check bits in half bus width mode)
- Up to 8 GB off-chip SDRAM
- Up to 2 memory ranks
- 1:2 frequency ratio mode
- Programmable support for 1T/2T memory command timing

- Automatic DDR3 low power mode operation through Hardware Low Power Interface
- Low area, low power architecture

2.2.2 DMA Controller for Low Speed Peripherals

The DMA LSP implements capability of direct data transfer between a low speed device, which is connected to a low speed peripheral interface, and memory without CPU usage.

It helps in maximizing system performance by decreasing a load of the SoC cores.

The DMA controller can only work in non-secure mode and has the following main features:

- Handshaking interface with two UARTs, two SPIs, and two I^2C controllers
- 8 channels, one per source and destination pair
- Unidirectional channels: data transfers in one direction only
- Multi-block transfers
- Single FIFO per channel for source and destination
- Automatic data packing or unpacking to fit FIFO width

2.2.3 Hardware Accelerator

Designed to improve the performance of computing, the hardware accelerator consists of hardware modules, which implement special algorithms of data processing.

2.3 System Control Module

The System Control Module is used to start the SoC and provide the initial configuration of all the SoC modules.

It contains the following main blocks:

- *Clock Control Unit* (**CCU**)
- Boot Controller
- I^2C Interface

CCU controls system clock and reset signals. It is responsible for generating valid clock signals for all integrated functional blocks, and disabling those blocks for power saving purposes.

Boot Controller is responsible for initial boot of the system. The following boot modes are provided:

- ROM mode – the core boots Baikal ROM Monitor software for the diagnostics and testing of the processor from the on-chip ROM
- FLASH mode – the core boots from an external FLASH memory through the external SPI interface

The boot SPI controller loads the executable code from the flash memory through the SPI interface after the processor reset. Connecting any other SPI devices to the controller is not recommended, as this may cause the SoC boot problems.

The I^2C Controller has limited functionality. In particular, registers of this controller are accessed only indirectly through the CCU registers. It is preferable to use two general purpose I^2C controllers.

2.4 High Speed Peripherals

2.4.1 PCIe Gen 3.0

The PCIe x4 interface contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the ***PCI Express Base Specification 3.0***.

PCIe provides the following main features:

- Up to x4 lanes (x1, x2, x4)
- Integrated PHY
- Transfer rates up to 8.0 GT/s (~1GB/s) per single lane
- PCIe *active state power management* (**ASPM**)
- PCIe *advanced error reporting* (**AER**) with Multiple Header Logging
- Internal Address Translation Unit
- Embedded multichannel DMA controller
- Automatic Lane Reversal
- ECRC Generation and Checking
- Maximum Payload Size 256 bytes
- 1 Virtual Channel
- 40-bit address width (XPA)

PCI legacy interrupts are not supported.

2.4.2 USB 2.0

The USB 2.0 controller is compatible with the xHCI specification by Intel Corporation.

It is optimized for the high-bandwidth applications and systems and supports the following device types:

- High-Speed (480 Mbps)
- Full-Speed (12 Mbps)
- Low-Speed (1.5 Mbps)

The controller supports the following general features:

- Single USB 2.0 port with 8-bit UTMI+ Low Pin Interface (ULPI) to an external PHY
- Embedded DMA controller
- Link Power Management (LPM) protocol
- Dynamic FIFO memory allocation for endpoints
- Keep-Alive feature in Low Speed mode and (micro-)SOFs in High Speed and Full Speed modes
- Hardware controlled USB bus level and packet level error handling
- Scattered data buffering
- Scattered packet support (Ethernet over USB application) to avoid software to copying and creating USB packets
- Descriptor caching and data pre-fetching
- Interrupt moderation
- 32-bit address width (non-XPA)

Since the address bus width is 32-bit, the controller does not support XPA. Thus, the embedded DMA controller supports physical memory addresses up to 4 GB.

2.4.3 SATA 6G

The SATA subsystem is an *Advanced Host Controller Interface* (**AHCI**) compliant *SATA Host Bus Adaptor* (**HBA**). Together with two PHYs, it forms two complete AHCI HBA interfaces.

The SATA subsystem supports the following features:

- SATA 1.5 Gb/s, SATA 3.0 Gb/s, and SATA 6.0 Gb/s speed negotiation
- Compliant with Serial ATA 3.2 and AHCI Revision 1.3.0 specifications
- 8b/10b encoding/decoding
- Power management features including automatic partial-to-slumber transition
- *Built-in self-test* (**BIST**) loopback modes
- Internal DMA engine per port
- 32-bit address width (non-XPA)

Since the address bus width is 32-bit, the controller does not support XPA. Thus, the internal DMA engines support physical memory addresses up to 4 GB.

2.4.4 10 Gb Ethernet

10 Gigabit Ethernet Media Access Controller (**XGMAC**) with integrated *10 Gigabit Ethernet Physical Coding Sublayer* (**XPCS**) and 10 Gigabit Ethernet *Physical Layer* (**PHY**) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gb/s Ethernet: 10GBASE-KX4 and 10GBASE-KR.

The XGMAC has the following main features:

- Full-duplex operation at 10 Gb/s
- Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard
- Full compliance with Clause 78 (Energy Efficient Ethernet (EEE) feature) of the IEEE 802.3az, standard for 10 Gbps operation
- Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames
- Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard
- Embedded DMA controller
- 40-bit address width (XPA)

2.4.5 1 Gb Ethernet

1 Gigabit Media Access Controller (**GMAC**) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

The GMAC has the following main features:

- 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY
- Full-duplex operation support
- Half-duplex operation support
- Separate transmission, reception, and control interfaces to the application
- Energy Efficient Ethernet (EEE) support
- Embedded DMA controller with independent Transmit and Receive engines
- 32-bit address width (non-XPA)

Since the address bus width is 32-bit, the controller does not support XPA. Thus, the embedded DMA controller supports physical memory addresses up to 4 GB.

2.5 Low Speed Peripherals

2.5.1 Peripheral Timers

The SoC contains three independent peripheral timers combined in a single controller.

Each peripheral timer is a 32-bit programmable timer supported “free-running” and “user-defined count” modes.

In “user-defined count” mode, a timer counts down from a programmed value and generates an interrupt when the count reaches zero. Timer interrupt can be detected even when the system bus clock is stopped.

2.5.2 GPIO

The SoC contains two GPIO controllers:

- 3-bit
- 32-bit

Both controllers support the following features:

- Independently controllable signals (3-bit or 32-bit accordingly)
- 2 separate registers (a data register and a data direction register) for each signal

To support interrupts to the Global Interrupt Controller, the GPIO*32 provides the following features:

- Independently configurable interrupt mode for each signal
- Combined interrupt status

The GPIO*3 does not support interrupts.

2.5.3 UART

The SoC contains two UARTs .

Each UART has a handshaking interface with the DMA LSP that can request and control data transfers between the UART and memory.

The UART contains registers used to control:

- Character length
- Baud rates up to 460.8 Kbps
- Parity generation/checking
- Interrupt generation

2.5.4 SPI

The SoC contains two SPI controllers.

The SPI controller is a full-duplex master or slave-synchronous serial interface used for short distance communication.

Each SPI has a handshaking interface with the DMA LSP that can request and control data transfers between the SPI and memory.

A master (a core or the DMA LSP controller) accesses data, control, and status information on the interface by using the SPI control and status registers.

The SPI controller operates as a serial master. It can connect to a serial-slave peripheral device using Motorola SPI interface.

2.5.5 I^2C

There SoC contains two general purpose I^2C controllers.

I^2C is a programmable serial interface that provides support for the communications link between the devices connected to the bus.

The I^2C controllers support the following features:

- Standard speed mode operation (up to 100 Kb/s)
- Master or Slave I^2C device operation
- Programmable 7- or 10-bit addressing
- 7- or 10-bit combined format transfers

Each I^2C has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the I^2C and memory.

2.6 System Monitoring

2.6.1 PVT Controller

Process, Voltage and Temperature (**PVT**) controller monitors the dual-core cluster subsystem.

It provides the following features:

- Measurement readiness is determined by polling data register or listening the interrupt line
- Programmable upper and lower threshold values for the measured PVT parameters to produce out-of-range interrupts
- Programmable timeout value for repetitive PVT parameters monitoring

2.6.2 Watchdog Timer

It is used to prevent system lockup that may be caused by software errors or hardware conflicts.

If a timeout occurs the *Watchdog timer* (**WDT**) can perform one of the following operations:

- Generates a system reset
- First generates an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generates a system reset

The generated interrupt is passed to the GIC. The generated reset is passed to the CCU, which in turn generates a reset for the components in the system. The WDT may be reset independently of other subsystems.

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification.

3.1 Power Supply Parameters

BE-T1000 requires four isolated voltage suppliers and a single unified ground supply as shown in the following table.

Table 3-1 BE-T1000 Power Domains

Package Pin Name	Voltage Supplied, V	Expected Maximum Current, A
VDD	0.95 (+/- 5%)	2.9
VPCI_09	0.95 (+/- 5%)	0.4
VXGB_09	0.95(+/- 5%)	0.6
VSATAP_09	0.95 (+/- 5%)	0.08
VSATATX_09	0.95 (+/- 5%)	0.05
VDDR_15	1.5 (+/- 5%)	0.4
VPCI_15	1.5 (+/- 5%)	0.1
VXGB_15	1.5 (+/- 5%)	0.2
VDDIO_18	1.8 (+ 10%, - 7%)	0.1
VSATA_18	1.8 (+ 10%, - 7%)	0.04
VDDR_18	1.8 (+ 10%, - 7%)	0.12
VPLLCORE_09	0.95 (+/- 5%)	0.01
VPLLDDR_09	0.95 (+/- 5%)	0.01
VPLLETH_09	0.95 (+/- 5%)	0.01
VPLLPCIE_09	0.95 (+/- 5%)	0.01
VPLLSATA_09	0.95 (+/- 5%)	0.01
VPVT_18	1.8 (+10%, -7%)	-
VSS	Ground	-
VSSIO	Ground	-
VSSCORE_PLL	Ground	-
VSSDDR_PLL	Ground	-
VSSETH_PLL	Ground	-
VSSPCIE_PLL	Ground	-
VSSSATA_PLL	Ground	-

3.2 Input Clocks

Reference clock characteristics are shown in the following table.

Table 3-2 BE-T1000 Reference Clock Characteristics

Description	Pin Names	Value	Unit	Note
Reference clock frequency	CLK25M	25	MHz	-
XGbE PHY reference clock frequency	XG_REF_CLKN[1], XG_REF_CLKP[1]	156.25	MHz	Differential pair Terminated[2] and unterminated[3] clocks
PCIe PHY reference clock frequency	PCIE_REF_CLKN[1], PCIE_REF_CLKP[1]	100	MHz	Differential pair Terminated[2] and unterminated[3] clocks
SATA PHY reference clock frequency	SATA_REFCLKP[1], SATA_REFCLKM[1]	100	MHz	Differential pair Terminated[2] and unterminated[3] clocks

NOTES:

1. If these pins are unused, they should be tied off to the ground potential
2. With terminated clocks, a 50 Ohms termination resistor is soldered on the board close to the SoC, preventing clock reflections while providing a clock source to the PHY
3. If the board clocks are unterminated, the clock's signal level will double as it hits the high-impedance input of the PHY reference clock inputs. This effect can also be used to provide a clean clock to the PHY, but ensure that the signal swing of the reference clock is not too high after doubling the amplitude

3.2.1 Reference Clock (CLK25M)

Table 3-3 Reference Clock (CLK25M) Requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable Stand-by current			15	uA

3.2.2 XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-4 XGbE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12 kHz to 20 MHz
Allowed jitter for 10GBASE-KX4			3.6	ps (rms)	Integrated from 12 kHz to 20 MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.3 PCIe PHY Reference Clock

Table 3-5 PCIe PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling

NOTE: 100 MHz is the only PCIe standard compliant refclk frequency. When using a 125 MHz refclk, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter

3.2.4 SATA PHY Reference Clock

Table 3-6 SATA PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Reference clock frequency offset	-350		350	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

Table 3-6 SATA PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

4 Processor Start and Reset

4.1 Processor Start Procedure

To start the processor, perform the following steps:

1. Supply voltage to the VDD, VPLLCORE_09, VPLLDDR_09, VPLLETH_09, VPLLPCIE_09, VPLLSATA_09, VPCI_09, VSATAP_09, VSATATX_09, VXGB_09 power domains (0.95V, as shown in Table 3-1)
2. **Wait for at least 20 ms**
3. Supply voltage to the VDDR_15, VPCI_15, VXGB_15 power domains (1.5V)
4. Supply voltage to the VDDIO_18, VDDR_18, VSATA_18 power domains (1.8V)
5. **Wait for at least 100 ms**
6. By this time, the clock signal on the CLK25M_IN input pin must be stabilized at a 25 MHz frequency

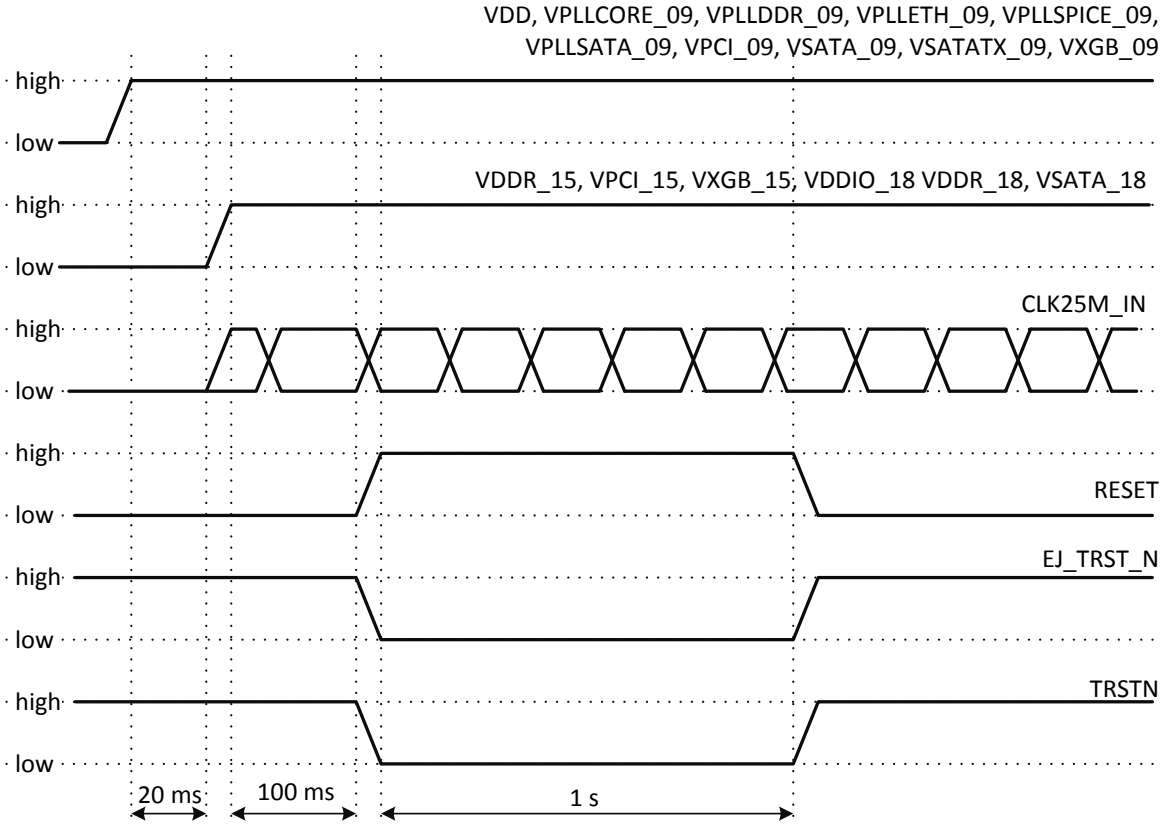

Figure 4-1 Start Sequence for BE-T1000

Once these steps are done, reset the processor as described in the next section.

4.2 Processor Reset Procedure

A stable 25 MHz clock signal at the CLK25M_IN pin is required to reset the processor.

To reset (restart) the processor, the following must be performed simultaneously on the RESET, EJ_TRST_N, and TRSTN inputs (see the figure below):

1. Hold RESET high for at least **1 s** and then keep it low

2. Hold EJ_TRST_N low for at least **1 s** and then keep it high
3. Hold TRSTN low for at least **1 s** and then keep it high

4.3 Boot Mode Selection

The BOOTCFG_0 and BOOTCFG_1 pins define boot mode during the whole reset sequence.

The current version of the processor supports two boot modes:

1. Normal mode as known as Flash Mode (software boots from an external flash memory through the SPI0 interface)
2. Debug mode as known as ROM Mode (a piece of diagnostic software—Baikal ROM Monitor—boots from the on-board ROM)

The BOOTCFG_0 pin must be connected to the ground in both cases. A low voltage (ground) on the BOOTCFG_1 pin selects the debug mode, while a high voltage (VDD) selects the normal mode (working software boots from an external flash memory).

5 Pin Assignment

5.1 Pinout List

The table below contains the list of I/O pins of the chip including the power-ground supplies.

Legend:

I	Input
O	Output
IO	In/Out
A	Analog
P	Power supply
G	Ground
NC	Not Connected

Table 5-1 Pinout List

	Ball ID	Package Pin name	Type	Description
1	AC3	BOOTCFG_0	I	Configuration strap pin: Boot mode
2	AC4	BOOTCFG_1	I	Configuration strap pin: Boot mode
3	R2	CLK25M_IN	I	PLL Reference Clock 25 MHz IN
4	R1	CLK25M_OUT	O	PLL Reference Clock 25 MHz OUT
5	K19	DDR_A[0]	O	SDRAM Address
6	K24	DDR_A[1]	O	SDRAM Address
7	H22	DDR_A[10]	O	SDRAM Address
8	M20	DDR_A[11]	O	SDRAM Address
9	K18	DDR_A[12]	O	SDRAM Address
10	M19	DDR_A[13]	O	SDRAM Address
11	L20	DDR_A[14]	O	SDRAM Address
12	J21	DDR_A[15]	O	SDRAM Address
13	K22	DDR_A[2]	O	SDRAM Address
14	M22	DDR_A[3]	O	SDRAM Address
15	M18	DDR_A[4]	O	SDRAM Address
16	P21	DDR_A[5]	O	SDRAM Address
17	N19	DDR_A[6]	O	SDRAM Address
18	P19	DDR_A[7]	O	SDRAM Address
19	P20	DDR_A[8]	O	SDRAM Address
20	M21	DDR_A[9]	O	SDRAM Address
21	V19	DDR_ATO	A	Analog Test Output (test Pad)
22	N22	DDR_BA[0]	O	SDRAM Bank Address
23	J19	DDR_BA[1]	O	SDRAM Bank Address

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
24	G20	DDR_BA[2]	O	SDRAM Bank Group
25	J22	DDR_CAS#	O	SDRAM CAS
26	M23	DDR_CK[0]	O	SDRAM Clock
27	L21	DDR_CK[1]	O	SDRAM Clock
28	M24	DDR_CK_N[0]	O	SDRAM Clock
29	L22	DDR_CK_N[1]	O	SDRAM Clock
30	K23	DDR_CKE[0]	O	SDRAM Clock enable
31	H20	DDR_CKE[1]	O	SDRAM Clock enable
32	H23	DDR_CS_N[0]	O	SDRAM Chip Select
33	J20	DDR_CS_N[1]	O	SDRAM Chip Select
34	AC22	DDR_DM[0]	O	SDRAM Data Mask
35	W21	DDR_DM[1]	O	SDRAM Data Mask
36	T22	DDR_DM[2]	O	SDRAM Data Mask
37	F22	DDR_DM[3]	O	SDRAM Data Mask
38	B22	DDR_DM[4]	O	SDRAM Data Mask
39	AA19	DDR_DQ[0]	IO	SDRAM Data
40	AA22	DDR_DQ[1]	IO	SDRAM Data
41	V24	DDR_DQ[10]	IO	SDRAM Data
42	Y22	DDR_DQ[11]	IO	SDRAM Data
43	Y21	DDR_DQ[12]	IO	SDRAM Data
44	AA24	DDR_DQ[13]	IO	SDRAM Data
45	AA23	DDR_DQ[14]	IO	SDRAM Data
46	V21	DDR_DQ[15]	IO	SDRAM Data
47	V20	DDR_DQ[16]	IO	SDRAM Data
48	P23	DDR_DQ[17]	IO	SDRAM Data
49	P24	DDR_DQ[18]	IO	SDRAM Data
50	R21	DDR_DQ[19]	IO	SDRAM Data
51	AB23	DDR_DQ[2]	IO	SDRAM Data
52	T21	DDR_DQ[20]	IO	SDRAM Data
53	U24	DDR_DQ[21]	IO	SDRAM Data
54	U21	DDR_DQ[22]	IO	SDRAM Data
55	T20	DDR_DQ[23]	IO	SDRAM Data
56	G21	DDR_DQ[24]	IO	SDRAM Data
57	E21	DDR_DQ[25]	IO	SDRAM Data

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
58	E22	DDR_DQ[26]	IO	SDRAM Data
59	E20	DDR_DQ[27]	IO	SDRAM Data
60	F21	DDR_DQ[28]	IO	SDRAM Data
61	E24	DDR_DQ[29]	IO	SDRAM Data
62	AB24	DDR_DQ[3]	IO	SDRAM Data
63	E23	DDR_DQ[30]	IO	SDRAM Data
64	F20	DDR_DQ[31]	IO	SDRAM Data
65	A21	DDR_DQ[32]	IO	SDRAM Data
66	B24	DDR_DQ[33]	IO	SDRAM Data
67	B21	DDR_DQ[34]	IO	SDRAM Data
68	B23	DDR_DQ[35]	IO	SDRAM Data
69	D21	DDR_DQ[36]	IO	SDRAM Data
70	D24	DDR_DQ[37]	IO	SDRAM Data
71	D23	DDR_DQ[38]	IO	SDRAM Data
72	D22	DDR_DQ[39]	IO	SDRAM Data
73	AD22	DDR_DQ[4]	IO	SDRAM Data
74	AA20	DDR_DQ[5]	IO	SDRAM Data
75	AD21	DDR_DQ[6]	IO	SDRAM Data
76	AA21	DDR_DQ[7]	IO	SDRAM Data
77	V22	DDR_DQ[8]	IO	SDRAM Data
78	V23	DDR_DQ[9]	IO	SDRAM Data
79	AC23	DDR_DQS[0]	IO	SDRAM Data Strobe
80	Y23	DDR_DQS[1]	IO	SDRAM Data Strobe
81	T23	DDR_DQS[2]	IO	SDRAM Data Strobe
82	F23	DDR_DQS[3]	IO	SDRAM Data Strobe
83	C23	DDR_DQS[4]	IO	SDRAM Data Strobe
84	AC24	DDR_DQS_N[0]	IO	SDRAM Data Strobe
85	Y24	DDR_DQS_N[1]	IO	SDRAM Data Strobe
86	T24	DDR_DQS_N[2]	IO	SDRAM Data Strobe
87	F24	DDR_DQS_N[3]	IO	SDRAM Data Strobe
88	C24	DDR_DQS_N[4]	IO	SDRAM Data Strobe
89	P18	DDR_DTO[0]	O	Digital Test Output (test Pad)
90	P17	DDR_DTO[1]	O	Digital Test Output (test Pad)
91	H24	DDR_ODT[0]	O	SDRAM On-Die termination

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
92	P22	DDR_ODT[1]	O	SDRAM On-Die termination
93	T19	DDR_RAM_RST_N	O	SDRAM Reset
94	H21	DDR_RAS#	O	SDRAM RAS
95	H17	DDR_VREF[0]	A	IO ring VREFI net
96	M17	DDR_VREF[1]	A	IO ring VREFI net
97	E18	DDR_VREF[2]	A	IO ring VREFI net
98	R18	DDR_VREF[3]	A	IO ring VREFI net
99	U18	DDR_VREF[4]	A	IO ring VREFI net
100	W19	DDR_VREF[5]	A	IO ring VREFI net
101	J18	DDR_VREFI_ZQ	A	IO ring VREFI ZQ net
102	G19	DDR_WE#	O	SDRAM WE
103	J17	DDR_ZQ	A	ZQ Resistor (to external calibration resistor)
104	A14	EJ_DINT_IN	I	DINT input
105	A13	EJ_TCK	I	Test clock input (TCK)
106	C14	EJ_TDI	I	TDI/TDO daisy-chain
107	C13	EJ_TDO	O	TDO
108	B14	EJ_TMS	I	Test mode select (TMS)
109	B13	EJ_TRST_N	I	Active-low test reset (TRST)
110	P7	G0_CLK_RX_I	I	RGMII Receive Clock
111	P6	G0_CLK_TX_I	O	RGMII Transmit Clock
112	N6	G0_GP_IN	I	GP input
113	N7	G0_GP_OUT	O	GP output
114	R5	G0_MDC	O	SMA Clock
115	R6	G0_MDIO	IO	SMA Data
116	R4	G0_RCTL_I	I	RGMII Receive Control
117	P2	G0_RXD_I[0]	I	RGMII Receive Data
118	P5	G0_RXD_I[1]	I	RGMII Receive Data
119	P1	G0_RXD_I[2]	I	RGMII Receive Data
120	R3	G0_RXD_I[3]	I	RGMII Receive Data
121	N1	G0_TCTL_O	O	RGMII Transmit Control
122	N2	G0_TXD_O[0]	O	RGMII Transmit Data
123	N3	G0_TXD_O[1]	O	RGMII Transmit Data
124	N4	G0_TXD_O[2]	O	RGMII Transmit Data
125	N5	G0_TXD_O[3]	O	RGMII Transmit Data

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
126	W1	G1_CLK_RX_I	I	RGMII Receive Clock
127	W2	G1_CLK_TX_I	O	RGMII Transmit Clock
128	Y1	G1_GP_IN	I	GP input
129	Y2	G1_GP_OUT	O	GP output
130	Y4	G1_MDC	O	SMA Clock
131	Y3	G1_MDIO	IO	SMA Data
132	Y5	G1_RCTL_I	I	RGMII Receive Control
133	U4	G1_RXD_I[0]	I	RGMII Receive Data
134	V6	G1_RXD_I[1]	I	RGMII Receive Data
135	V4	G1_RXD_I[2]	I	RGMII Receive Data
136	V5	G1_RXD_I[3]	I	RGMII Receive Data
137	V2	G1_TCTL_O	O	RGMII Transmit Control
138	T5	G1_TXD_O[0]	O	RGMII Transmit Data
139	T6	G1_TXD_O[1]	O	RGMII Transmit Data
140	U5	G1_TXD_O[2]	O	RGMII Transmit Data
141	V1	G1_TXD_O[3]	O	RGMII Transmit Data
142	F9	GPIO[0]	IO	GPIO Data / GMAC1 timestamp function
143	F8	GPIO[1]	IO	GPIO Data / GMAC2 timestamp function
144	D1	GPIO[10]	IO	GPIO Data
145	C5	GPIO[11]	IO	GPIO Data
146	C3	GPIO[12]	IO	GPIO Data
147	C2	GPIO[13]	IO	GPIO Data
148	B5	GPIO[14]	IO	GPIO Data
149	B3	GPIO[15]	IO	GPIO Data
150	E3	GPIO[16]	IO	GPIO Data
151	B2	GPIO[17]	IO	GPIO Data
152	C1	GPIO[18]	IO	GPIO Data
153	A2	GPIO[19]	IO	GPIO Data
154	F7	GPIO[2]	IO	GPIO Data / PCIe device enable
155	A4	GPIO[20]	IO	GPIO Data
156	B4	GPIO[21]	IO	GPIO Data
157	A3	GPIO[22]	IO	GPIO Data
158	B6	GPIO[23]	IO	GPIO Data
159	A6	GPIO[24]	IO	GPIO Data

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
160	F10	GPIO[25]	IO	GPIO Data
161	E8	GPIO[26]	IO	GPIO Data
162	E7	GPIO[27]	IO	GPIO Data
163	B7	GPIO[28]	IO	GPIO Data
164	A7	GPIO[29]	IO	GPIO Data
165	E6	GPIO[3]	IO	GPIO Data / Crypto device enable
166	E9	GPIO[30]	IO	GPIO Data
167	D8	GPIO[31]	IO	GPIO Data
168	E5	GPIO[4]	IO	GPIO Data
169	E4	GPIO[5]	IO	GPIO Data
170	D5	GPIO[6]	IO	GPIO Data
171	D3	GPIO[7]	IO	GPIO Data
172	A5	GPIO[8]	IO	GPIO Data
173	D2	GPIO[9]	IO	GPIO Data
174	W7	GPIO3[0]	IO	GPIO Data
175	W6	GPIO3[1]	IO	GPIO Data
176	W5	GPIO3[2]	IO	GPIO Data
177	G17	GPVT	A	Filter connection pin. **Note that there is no GPVT connection to the board power supply**
178	AD5	I2C0_SCL	IO	I^2C clock
179	AD4	I2C0_SDA	IO	I^2C data
180	K7	I2C1_SCL	IO	I^2C1 clock
181	K6	I2C1_SDA	IO	I^2C1 data
182	J1	I2C2_SCL	IO	I^2C2 clock
183	K1	I2C2_SDA	IO	I^2C2 data
184	R7	MBIST_CLK	I	MBIST clock
185	AA11	NC	NC	Not connected
186	AB11	NC	NC	Not connected
187	AC11	NC	NC	Not connected
188	AC21	NC	NC	Not connected
189	AD1	NC	NC	Not connected
190	AD11	NC	NC	Not connected
191	D18	NC	NC	Not connected
192	D19	NC	NC	Not connected
193	F16	NC	NC	Not connected

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
194	G18	NC	NC	Not connected
195	K17	NC	NC	Not connected
196	L17	NC	NC	Not connected
197	R17	NC	NC	Not connected
198	T18	NC	NC	Not connected
199	AC5	PCIE_AMON	O	Analog monitor bump
200	AD20	PCIE_ATT_BUT	I	Attention button pressed
201	V17	PCIE_ATT_IND[0]	O	Controls the system attention indicator
202	T17	PCIE_ATT_IND[1]	O	Controls the system attention indicator
203	AA18	PCIE_CMD_INT	I	Hot-plug controller command completed interrupt
204	W13	PCIE_DMON	O	Differential digital monitor bump
205	W15	PCIE_DMONB	O	Differential digital monitor bump
206	V18	PCIE_INTRL_CTRL	O	Electromechanical Interlock Control
207	W18	PCIE_INTRL_ENG	I	System Electromechanical Interlock Engaged
208	W16	PCIE_MRL_SENS	I	MRL sensor state
209	AD19	PCIE_PRES_ST	I	Presence detect state
210	AA17	PCIE_PWR_CTRL	O	Controls the system power controller
211	AB18	PCIE_PWR_FAULT	I	Power fault detect
212	Y18	PCIE_PWR_IND[0]	O	Controls the system power indicator
213	U17	PCIE_PWR_IND[1]	O	Controls the system power indicator
214	W12	PCIE_RBIAS	IO	Bias resistor bump
215	AD14	PCIE_REF_CLKN	I	Differential reference clocks from pads
216	AC14	PCIE_REF_CLKP	I	Differential reference clocks from pads
217	AD12	PCIE_RXM[0]	I	Receive data diff pair
218	AD13	PCIE_RXM[1]	I	Receive data diff pair
219	AD15	PCIE_RXM[2]	I	Receive data diff pair
220	AD16	PCIE_RXM[3]	I	Receive data diff pair
221	AC12	PCIE_RXP[0]	I	Receive data diff pair
222	AC13	PCIE_RXP[1]	I	Receive data diff pair
223	AC15	PCIE_RXP[2]	I	Receive data diff pair
224	AC16	PCIE_RXP[3]	I	Receive data diff pair
225	AA12	PCIE_TXM[0]	O	Transmit data diff pair
226	AA13	PCIE_TXM[1]	O	Transmit data diff pair
227	AA15	PCIE_TXM[2]	O	Transmit data diff pair

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
228	AA16	PCIE_TXM[3]	O	Transmit data diff pair
229	Y12	PCIE_TXP[0]	O	Transmit data diff pair
230	Y13	PCIE_TXP[1]	O	Transmit data diff pair
231	Y15	PCIE_TXP[2]	O	Transmit data diff pair
232	Y16	PCIE_TXP[3]	O	Transmit data diff pair
233	U6	RES_3		Reserved
234	T1	RESET	I	System Reset
235	C15	SATA_P0CPDET	I	Cold Presence Detect P0
236	E15	SATA_P0CPPOD	O	Cold Presence Power-On Device P0
237	F15	SATA_P0MPSWITCH	I	Mechanical Presence Switch P0
238	E14	SATA_P1CPDET	I	Cold Presence Detect P1
239	D15	SATA_P1CPPOD	O	Cold Presence Power-On Device P1
240	D14	SATA_P1MPSWITCH	I	Mechanical Presence Switch P1
241	A20	SATA_REFCLKM	I	Reference clock diff pair
242	B20	SATA_REFCLKP	I	Reference clock diff pair
243	C19	SATA_RESREF	A	Reference Resistor
244	B19	SATA_RXM[0]	I	Receive data diff pair port 0
245	B17	SATA_RXM[1]	I	Receive data diff pair port 1
246	A19	SATA_RXP[0]	I	Receive data diff pair port 0
247	A17	SATA_RXP[1]	I	Receive data diff pair port 1
248	B18	SATA_TXM[0]	O	Transmit data diff pair port 0
249	B16	SATA_TXM[1]	O	Transmit data diff pair port 1
250	A18	SATA_TXP[0]	O	Transmit data diff pair port 0
251	A16	SATA_TXP[1]	O	Transmit data diff pair port 1
252	J7	SPI0_RXD	I	Receive data
253	H6	SPI0_SCLK_OUT	O	Output Clock
254	H7	SPI0_SS_N	O	Slave Select
255	J6	SPI0_TXD	O	Transmit data
256	F6	SPI1_RXD	I	Receive data
257	F2	SPI1_SCLK_OUT	O	Output Clock
258	F1	SPI1_SS_N[0]	O	Slave Select
259	G5	SPI1_SS_N[1]	O	Slave Select
260	G6	SPI1_SS_N[2]	O	Slave Select
261	G7	SPI1_SS_N[3]	O	Slave Select

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
262	F5	SPI1_TXD	O	Transmit data
263	H5	SPI2_RXD	I	Receive data
264	H1	SPI2_SCLK_OUT	O	Output Clock
265	G4	SPI2_SS_N[0]	O	Slave Select
266	G1	SPI2_SS_N[1]	O	Slave Select
267	G2	SPI2_SS_N[2]	O	Slave Select
268	G3	SPI2_SS_N[3]	O	Slave Select
269	H2	SPI2_TXD	O	Transmit data
270	AA1	TCK	I	Test clock
271	AB2	TDI	I	Test data in
272	AB1	TDO	O	Test data out
273	F14	TEST	I	Test pin
274	AA2	TMS	I	Test mode select
275	F13	TR_CLK	O	Trace clock output to probe
276	A9	TR_DATA[0]	O	Trace data output to External Probe
277	B9	TR_DATA[1]	O	Trace data output to External Probe
278	C9	TR_DATA[10]	O	Trace data output to External Probe
279	A10	TR_DATA[11]	O	Trace data output to External Probe
280	C11	TR_DATA[12]	O	Trace data output to External Probe
281	B12	TR_DATA[13]	O	Trace data output to External Probe
282	E12	TR_DATA[14]	O	Trace data output to External Probe
283	A12	TR_DATA[15]	O	Trace data output to External Probe
284	C8	TR_DATA[2]	O	Trace data output to External Probe
285	E10	TR_DATA[3]	O	Trace data output to External Probe
286	E11	TR_DATA[4]	O	Trace data output to External Probe
287	D9	TR_DATA[5]	O	Trace data output to External Probe
288	B10	TR_DATA[6]	O	Trace data output to External Probe
289	F11	TR_DATA[7]	O	Trace data output to External Probe
290	F12	TR_DATA[8]	O	Trace data output to External Probe
291	D11	TR_DATA[9]	O	Trace data output to External Probe
292	B11	TR_DM	O	Debug Mode indicator to External Probe
293	E13	TR_PROBE_N	I	PIB (clock/data) enable signal from probe
294	D13	TR_TRIGIN	I	Trigger input coming from probe
295	A11	TR_TRIGOUT	O	Trigger output going to probe

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
296	AA5	TRSTN	I	Test reset
297	U7	TSTSEL_1	I	Func/MBIST mode selection. Bit_1
298	T7	TSTSEL_2	I	Func/MBIST mode selection. Bit_2
299	U3	TSTSEL_3	I	Boot frequency selection
300	J4	UART0_RXD	I	Receive data
301	J5	UART0_TXD	O	Transmit data
302	J2	UART1_RXD	I	Receive data
303	J3	UART1_TXD	O	Transmit data
304	K2	ULPI_CLK	I	ULPI Clock
305	L1	ULPI_DATA[0]	IO	ULPI Data
306	L2	ULPI_DATA[1]	IO	ULPI Data
307	L5	ULPI_DATA[2]	IO	ULPI Data
308	M5	ULPI_DATA[3]	IO	ULPI Data
309	M6	ULPI_DATA[4]	IO	ULPI Data
310	M7	ULPI_DATA[5]	IO	ULPI Data
311	M3	ULPI_DATA[6]	IO	ULPI Data
312	M4	ULPI_DATA[7]	IO	ULPI Data
313	K3	ULPI_DIR	I	ULPI Data Bus Control
314	K4	ULPI_NXT	I	ULPI Next Data Control
315	L6	ULPI_STP	O	ULPI Stop Output Control
316	K5	USB2_OVER	I	Overcurrent indication of the root port
317	L7	USB2_VBUS	O	Port Power control for Downstream port
318	Y8	XG_AMON	O	Analog monitor bump
319	W10	XG_DMON	O	Differential digital monitor bump
320	W11	XG_DMONB	O	Differential digital monitor bump
321	W8	XG_RBIAS	IO	Bias resistor bump
322	AD8	XG_REF_CLKN	I	Differential reference clocks from pads (unused)
323	AC8	XG_REF_CLKP	I	Differential reference clocks from pads (unused)
324	AD6	XG_RXM[0]	I	Receive data diff pair
325	AD7	XG_RXM[1]	I	Receive data diff pair
326	AD10	XG_RXM[2]	I	Receive data diff pair
327	AD9	XG_RXM[3]	I	Receive data diff pair
328	AC6	XG_RXP[0]	I	Receive data diff pair
329	AC7	XG_RXP[1]	I	Receive data diff pair

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
330	AC10	XG_RXP[2]	I	Receive data diff pair
331	AC9	XG_RXP[3]	I	Receive data diff pair
332	AA6	XG_TXM[0]	O	Transmit data diff pair
333	AA7	XG_TXM[1]	O	Transmit data diff pair
334	AA10	XG_TXM[2]	O	Transmit data diff pair
335	AA9	XG_TXM[3]	O	Transmit data diff pair
336	Y6	XG_TXP[0]	O	Transmit data diff pair
337	Y7	XG_TXP[1]	O	Transmit data diff pair
338	Y10	XG_TXP[2]	O	Transmit data diff pair
339	Y9	XG_TXP[3]	O	Transmit data diff pair
340	A1	VDD	P	Core power
341	A15	VDD	P	Core power
342	A22	VDD	P	Core power
343	A8	VDD	P	Core power
344	AB4	VDD	P	Core power
345	AC1	VDD	P	Core power
346	AC19	VDD	P	Core power
347	AC20	VDD	P	Core power
348	E1	VDD	P	Core power
349	E16	VDD	P	Core power
350	G10	VDD	P	Core power
351	G11	VDD	P	Core power
352	G12	VDD	P	Core power
353	G13	VDD	P	Core power
354	G14	VDD	P	Core power
355	G15	VDD	P	Core power
356	G16	VDD	P	Core power
357	G22	VDD	P	Core power
358	G8	VDD	P	Core power
359	G9	VDD	P	Core power
360	J10	VDD	P	Core power
361	J11	VDD	P	Core power
362	J12	VDD	P	Core power
363	J13	VDD	P	Core power

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
364	J14	VDD	P	Core power
365	J15	VDD	P	Core power
366	J16	VDD	P	Core power
367	J8	VDD	P	Core power
368	J9	VDD	P	Core power
369	L10	VDD	P	Core power
370	L11	VDD	P	Core power
371	L12	VDD	P	Core power
372	L13	VDD	P	Core power
373	L14	VDD	P	Core power
374	L15	VDD	P	Core power
375	L16	VDD	P	Core power
376	L8	VDD	P	Core power
377	L9	VDD	P	Core power
378	M1	VDD	P	Core power
379	N10	VDD	P	Core power
380	N11	VDD	P	Core power
381	N12	VDD	P	Core power
382	N13	VDD	P	Core power
383	N14	VDD	P	Core power
384	N15	VDD	P	Core power
385	N16	VDD	P	Core power
386	N8	VDD	P	Core power
387	N9	VDD	P	Core power
388	R10	VDD	P	Core power
389	R11	VDD	P	Core power
390	R12	VDD	P	Core power
391	R13	VDD	P	Core power
392	R14	VDD	P	Core power
393	R15	VDD	P	Core power
394	R16	VDD	P	Core power
395	R22	VDD	P	Core power
396	R8	VDD	P	Core power
397	R9	VDD	P	Core power

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
398	U10	VDD	P	Core power
399	U11	VDD	P	Core power
400	U12	VDD	P	Core power
401	U13	VDD	P	Core power
402	U14	VDD	P	Core power
403	U15	VDD	P	Core power
404	U16	VDD	P	Core power
405	U8	VDD	P	Core power
406	U9	VDD	P	Core power
407	V3	VDD	P	Core power
408	W22	VDD	P	Core power
409	AB3	VDDIO_18	P	IO power
410	C10	VDDIO_18	P	IO power
411	C12	VDDIO_18	P	IO power
412	C4	VDDIO_18	P	IO power
413	C6	VDDIO_18	P	IO power
414	C7	VDDIO_18	P	IO power
415	F3	VDDIO_18	P	IO power
416	H3	VDDIO_18	P	IO power
417	L3	VDDIO_18	P	IO power
418	P3	VDDIO_18	P	IO power
419	T3	VDDIO_18	P	IO power
420	W3	VDDIO_18	P	IO power
421	Y17	VDDIO_18	P	IO power
422	AB22	VDDR_15	P	VDDQ voltage supply
423	C22	VDDR_15	P	VDDQ voltage supply
424	D20	VDDR_15	P	VDDQ voltage supply
425	F19	VDDR_15	P	VDDQ voltage supply
426	H19	VDDR_15	P	VDDQ voltage supply
427	J24	VDDR_15	P	VDDQ voltage supply
428	K21	VDDR_15	P	VDDQ voltage supply
429	L19	VDDR_15	P	VDDQ voltage supply
430	L24	VDDR_15	P	VDDQ voltage supply
431	N18	VDDR_15	P	VDDQ voltage supply

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
432	N21	VDDR_15	P	VDDQ voltage supply
433	N24	VDDR_15	P	VDDQ voltage supply
434	R20	VDDR_15	P	VDDQ voltage supply
435	U20	VDDR_15	P	VDDQ voltage supply
436	U23	VDDR_15	P	VDDQ voltage supply
437	Y20	VDDR_15	P	VDDQ voltage supply
438	A24	VDDR_18	P	PLL power supply
439	AD24	VDDR_18	P	PLL power supply
440	G24	VDDR_18	P	PLL power supply
441	R24	VDDR_18	P	PLL power supply
442	W24	VDDR_18	P	PLL power supply
443	AA14	VPCI_09	P	PCIe PHY analog 0.95V
444	AB13	VPCI_09	P	PCIe PHY analog 0.95V
445	AB16	VPCI_09	P	PCIe PHY analog 0.95V
446	Y14	VPCI_15	P	PCIe PHY IO 1.5V
447	U1	VPLLCORE_09	P	PLL power
448	AD18	VPLLDDR_09	P	PLL power
449	AD3	VPLLETH_09	P	PLL power
450	AD17	VPLLPCIE_09	P	PLL power
451	D17	VPLLSATA_09	P	PLL power
452	F17	VPVT_18	P	Analog power for PVT sensor (1.8V)
453	V7	VQPS	P	0V or floating or 1.8V +/- 10%
454	C20	VSATA_18	P	SATA PHY High-voltage power supply
455	C17	VSATAP_09	P	SATA PHY analog and digital supply
456	C18	VSATATX_09	P	SATA PHY transmit supply
457	A23	VSS	G	VSSQ ground
458	AA3	VSS	G	Core ground
459	AB12	VSS	G	Core ground
460	AB14	VSS	G	Core ground
461	AB15	VSS	G	Core ground
462	AB17	VSS	G	Core ground
463	AB19	VSS	G	VSSQ ground
464	AB20	VSS	G	VSSQ ground
465	AB21	VSS	G	VSSQ ground

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
466	AB5	VSS	G	XGbE ground
467	AB7	VSS	G	XGbE ground
468	AB9	VSS	G	XGbE ground
469	AD2	VSS	G	Core ground
470	AD23	VSS	G	VSSQ ground
471	B1	VSS	G	Core ground
472	B15	VSS	G	Core ground
473	B8	VSS	G	Core ground
474	C16	VSS	G	SATA GD (PHY ground)
475	C21	VSS	G	VSSQ ground
476	E17	VSS	G	PCIe ground
477	E19	VSS	G	Core ground
478	E2	VSS	G	Core ground
479	F18	VSS	G	VSSQ ground
480	G23	VSS	G	VSSQ ground
481	H10	VSS	G	Core ground
482	H11	VSS	G	Core ground
483	H12	VSS	G	PCIe ground
484	H13	VSS	G	Core ground
485	H14	VSS	G	PCIe ground
486	H15	VSS	G	PCIe ground
487	H16	VSS	G	Core ground
488	H18	VSS	G	VSSQ ground
489	H8	VSS	G	Core ground
490	H9	VSS	G	Core ground
491	J23	VSS	G	VSSQ ground
492	K10	VSS	G	Core ground
493	K11	VSS	G	Core ground
494	K12	VSS	G	Core ground
495	K13	VSS	G	Core ground
496	K14	VSS	G	PCIe ground
497	K15	VSS	G	Core ground
498	K16	VSS	G	Core ground
499	K20	VSS	G	VSSQ ground

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
500	K8	VSS	G	Core ground
501	K9	VSS	G	Core ground
502	L18	VSS	G	VSSQ ground
503	L23	VSS	G	VSSQ ground
504	M10	VSS	G	Core ground
505	M11	VSS	G	Core ground
506	M12	VSS	G	Core ground
507	M13	VSS	G	Core ground
508	M14	VSS	G	Core ground
509	M15	VSS	G	Core ground
510	M16	VSS	G	Core ground
511	M2	VSS	G	Core ground
512	M8	VSS	G	Core ground
513	M9	VSS	G	Core ground
514	N17	VSS	G	VSSQ ground
515	N20	VSS	G	VSSQ ground
516	N23	VSS	G	VSSQ ground
517	P10	VSS	G	Core ground
518	P11	VSS	G	Core ground
519	P12	VSS	G	Core ground
520	P13	VSS	G	Core ground
521	P14	VSS	G	Core ground
522	P15	VSS	G	Core ground
523	P16	VSS	G	Core ground
524	P8	VSS	G	Core ground
525	P9	VSS	G	Core ground
526	R19	VSS	G	VSSQ ground
527	R23	VSS	G	VSSQ ground
528	T10	VSS	G	Core ground
529	T11	VSS	G	Core ground
530	T12	VSS	G	Core ground
531	T13	VSS	G	Core ground
532	T14	VSS	G	Core ground
533	T15	VSS	G	Core ground

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
534	T16	VSS	G	Core ground
535	T8	VSS	G	Core ground
536	T9	VSS	G	Core ground
537	U19	VSS	G	VSSQ ground
538	U2	VSS	G	Core ground
539	U22	VSS	G	VSSQ ground
540	V10	VSS	G	Core ground
541	V11	VSS	G	Core ground
542	V12	VSS	G	Core ground
543	V13	VSS	G	Core ground
544	V14	VSS	G	Core ground
545	V15	VSS	G	Core ground
546	V16	VSS	G	Core ground
547	V8	VSS	G	Core ground
548	V9	VSS	G	Core ground
549	W14	VSS	G	Core ground
550	W20	VSS	G	VSSQ ground
551	W23	VSS	G	VSSQ ground
552	W9	VSS	G	XGbE ground
553	Y11	VSS	G	XGbE ground
554	Y19	VSS	G	VSSQ ground
555	T2	VSSCORE_PLL	G	PLL ground
556	AC18	VSSDDR_PLL	G	PLL ground
557	AC2	VSSETH_PLL	G	PLL ground
558	AA4	VSSIO	G	IO ground
559	D10	VSSIO	G	IO ground
560	D12	VSSIO	G	IO ground
561	D4	VSSIO	G	IO ground
562	D6	VSSIO	G	IO ground
563	D7	VSSIO	G	IO ground
564	F4	VSSIO	G	IO ground
565	H4	VSSIO	G	IO ground
566	L4	VSSIO	G	IO ground
567	P4	VSSIO	G	IO ground

Table 5-1 Pinout List (continued)

	Ball ID	Package Pin name	Type	Description
568	T4	VSSIO	G	IO ground
569	W17	VSSIO	G	IO ground
570	W4	VSSIO	G	IO ground
571	AC17	VSSPCIE_PLL	G	PLL ground
572	D16	VSSSATA_PLL	G	PLL ground
573	AB10	VXGB_09	P	XGbE PHY analog 0.95V
574	AB6	VXGB_09	P	XGbE PHY analog 0.95V
575	AB8	VXGB_09	P	XGbE PHY analog 0.95V
576	AA8	VXGB_15	P	XGbE PHY IO 1.5V

5.2 Package Ball Map

The diagrams below show pinout from the top view of the package.

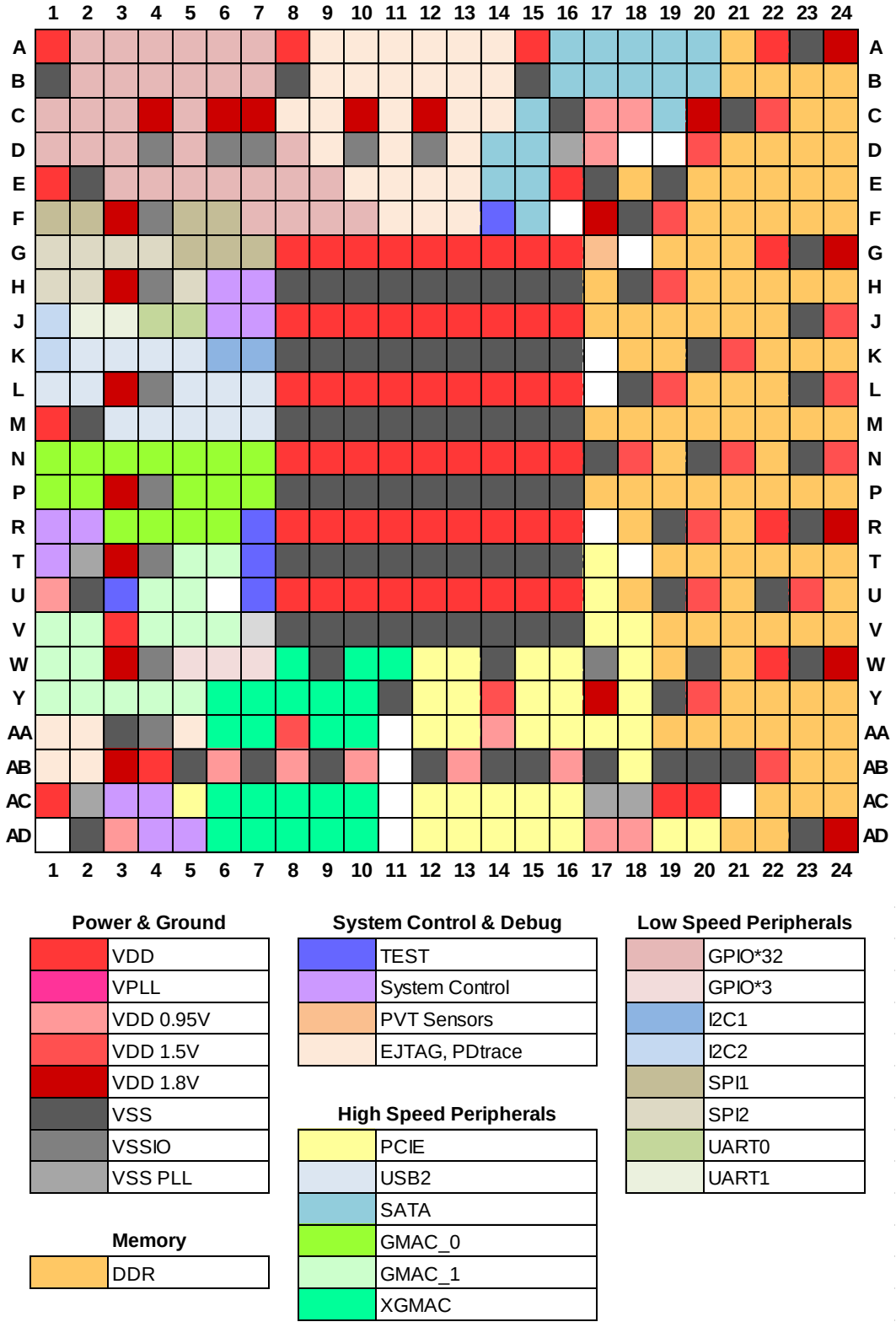

Figure 5-1 Ball Map

5.2.1 Power and Ground

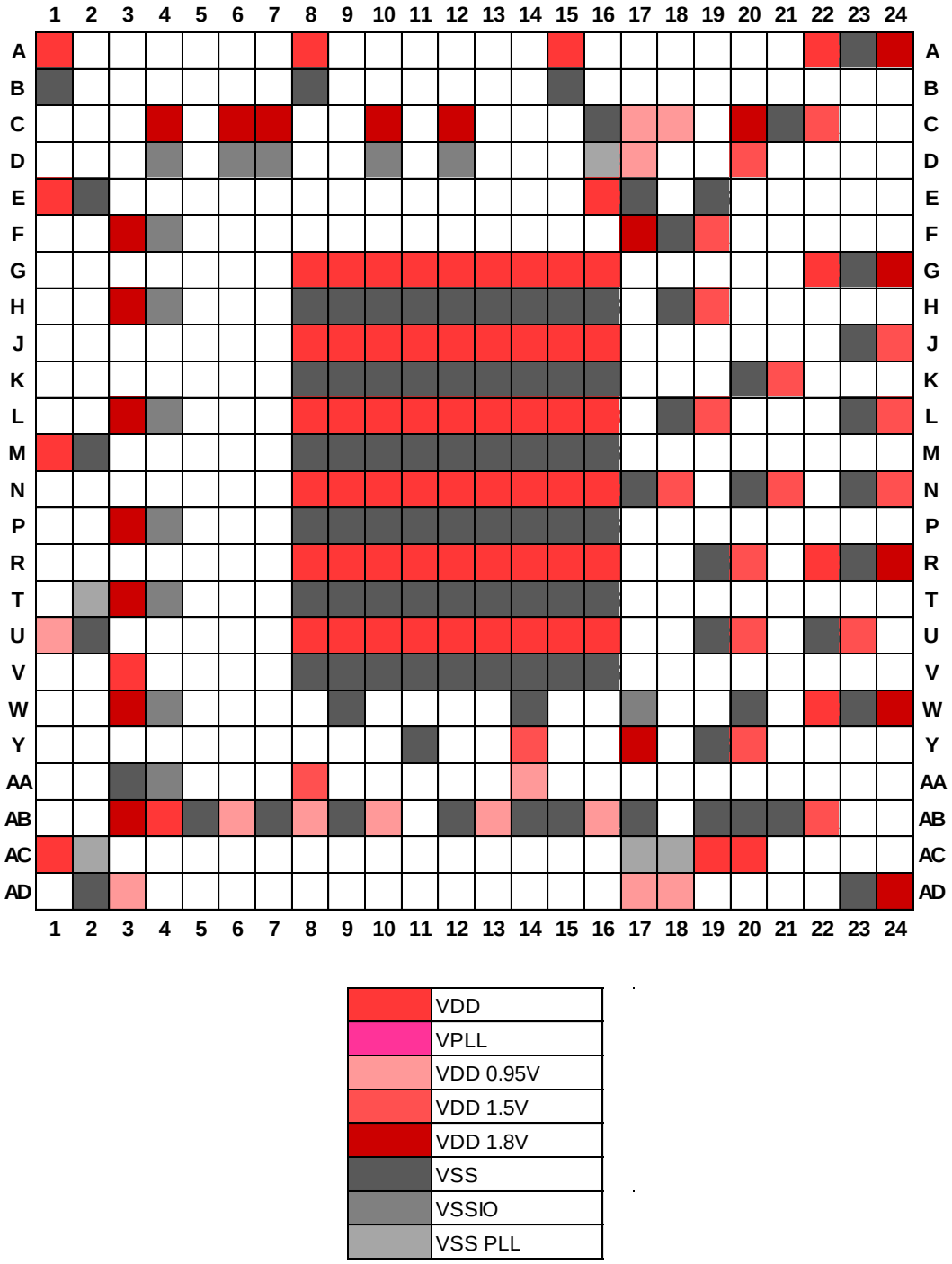

Figure 5-2 Power and Ground Pin Placement

5.2.2 High Speed Peripherals

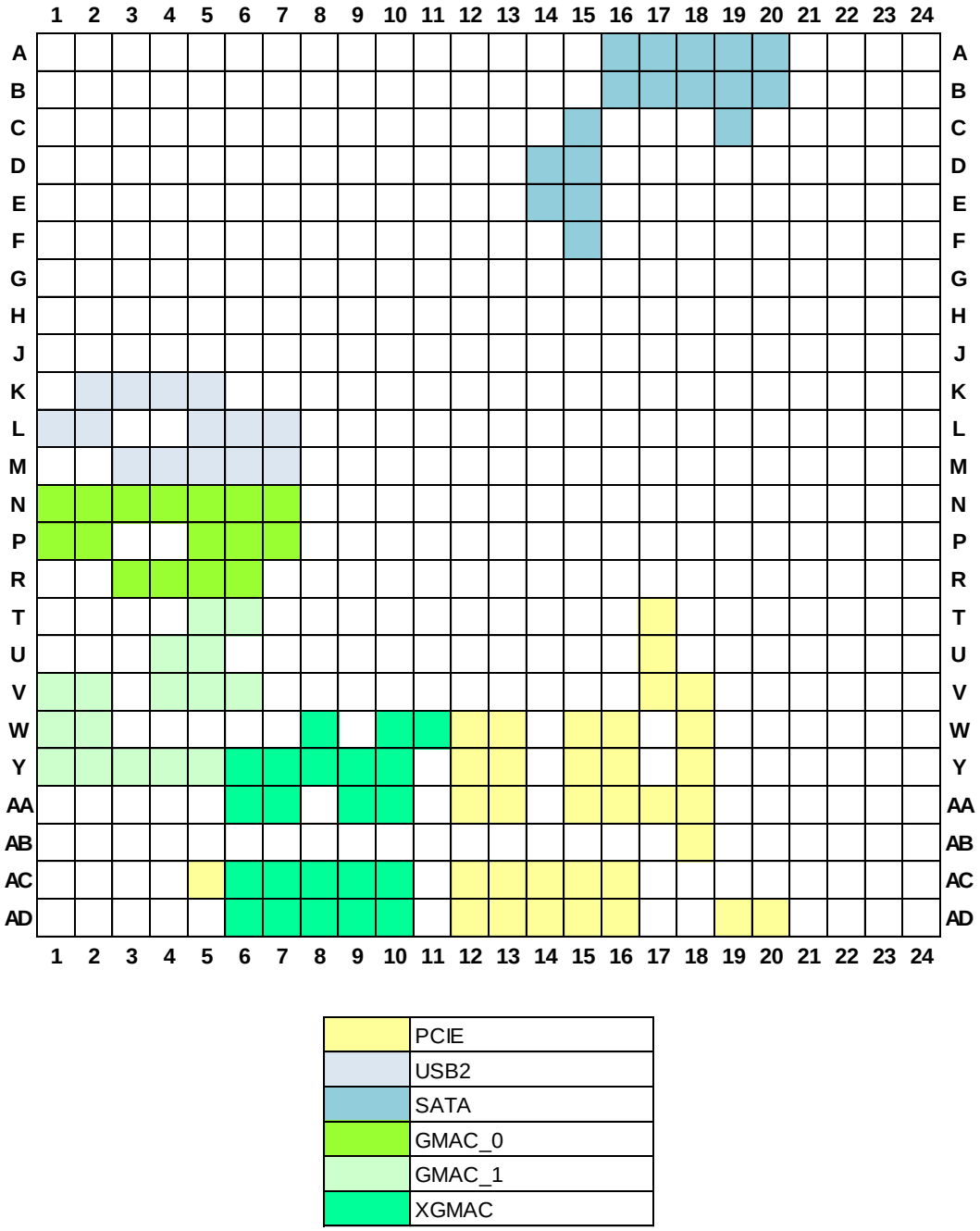

Figure 5-3 High Speed Peripherals Pin Placement

5.2.3 Low Speed Peripherals

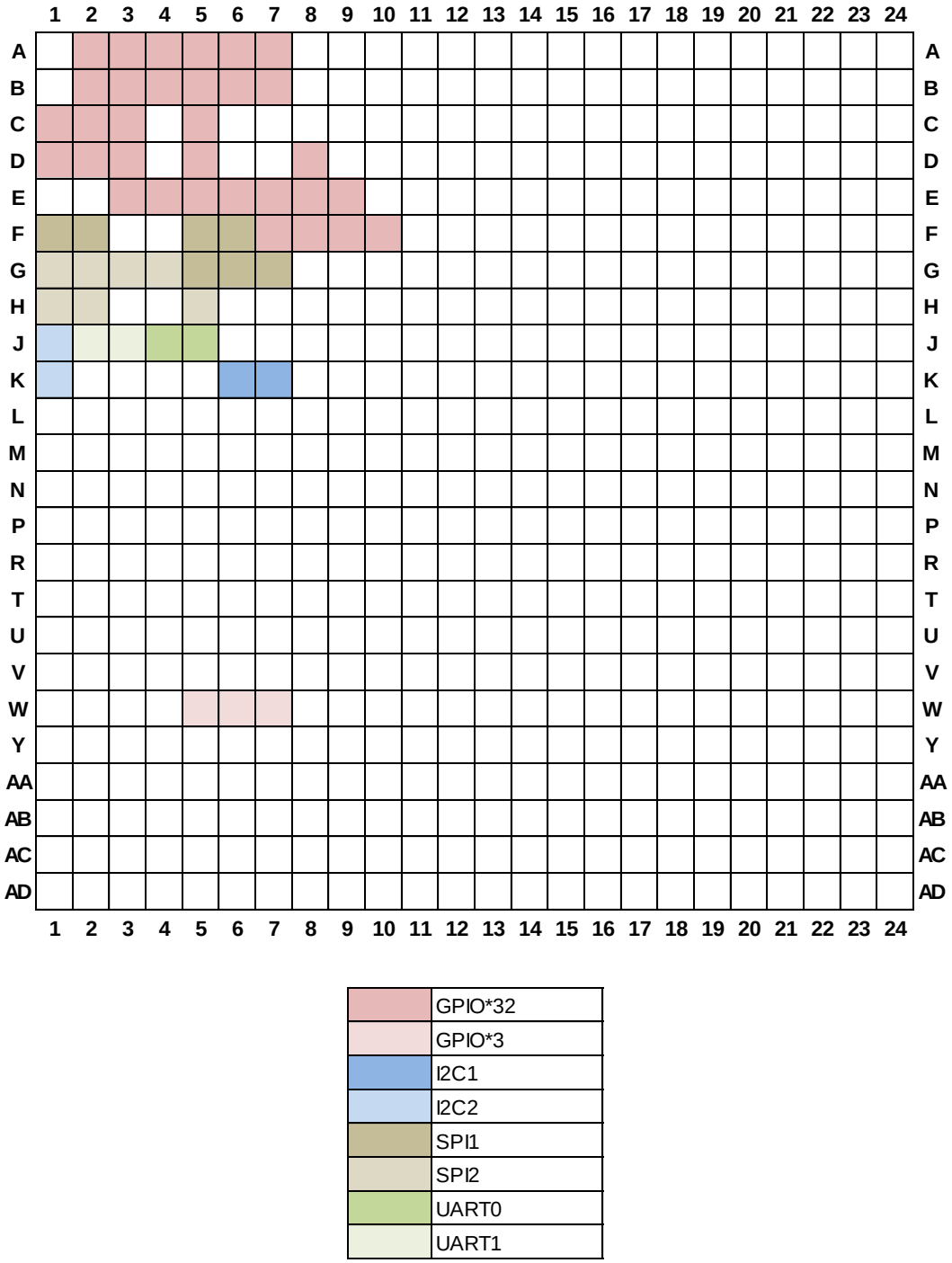

Figure 5-4 Low Speed Peripherals Pin Placement

5.2.4 Memory

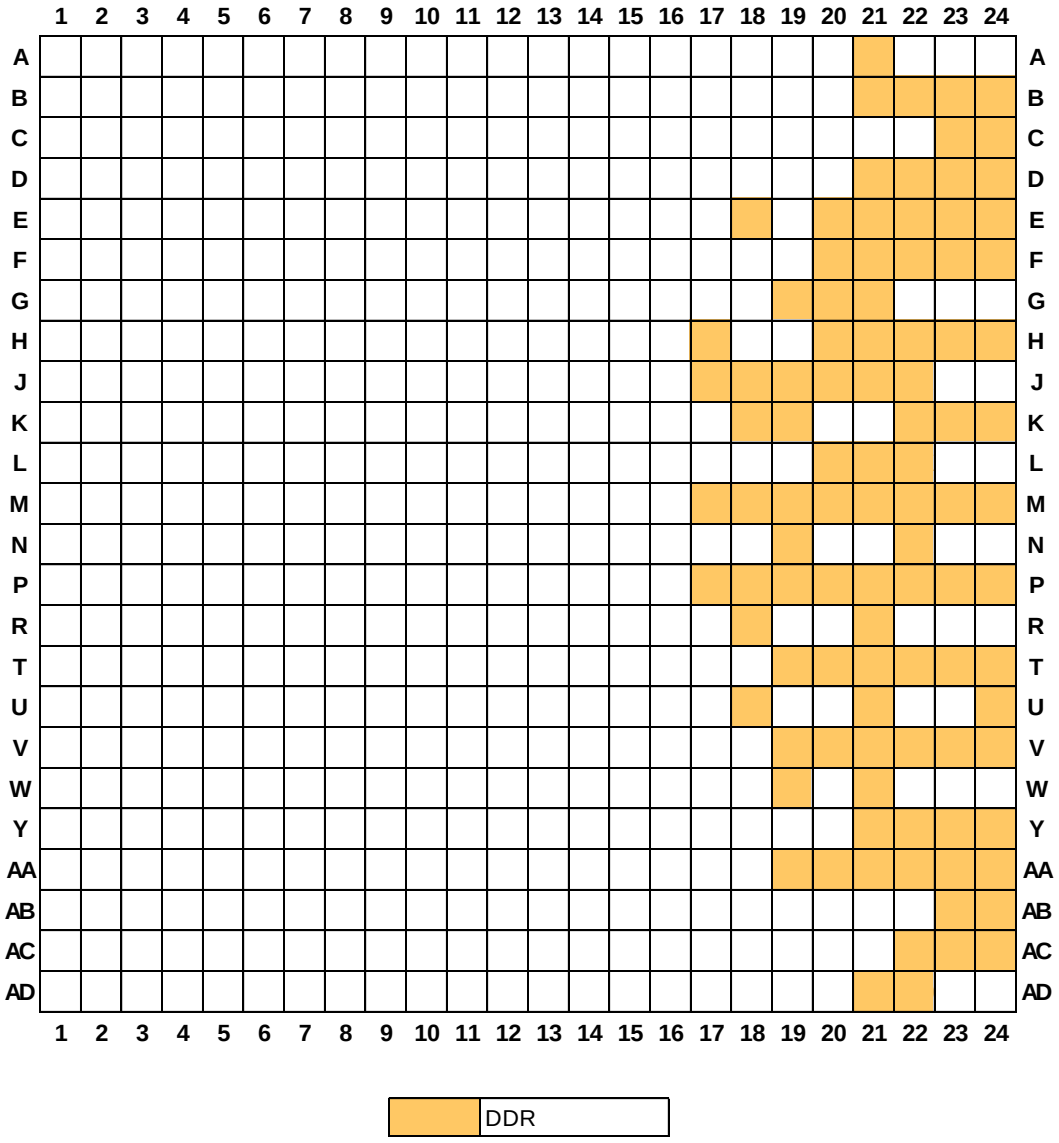

Figure 5-5 Memory Pin Placement

5.2.5 System Control and Debug

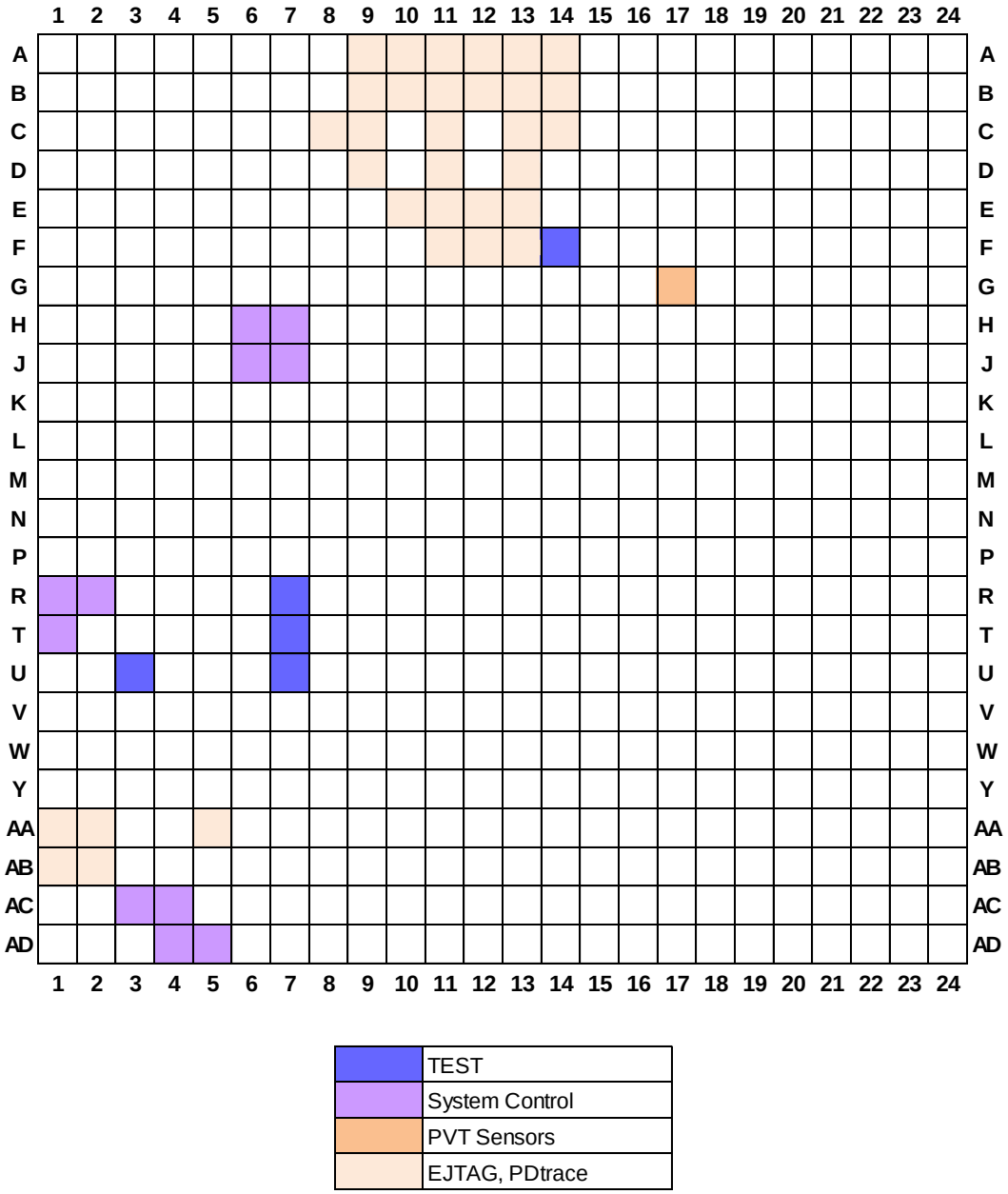

Figure 5-6 System Control and Debug Pin Placement

6 Package

6.1 Package Parameters

The main package parameters are specified in the following table.

Table 6-1 BE-T1000 Main Package Parameters

Description	Value
Package dimensions	25x25 mm
Number of interconnects	576
Ball pitch	1 mm
Ball diameter	0.6 ± 0.1 mm
Module height (min / nominal / max)	2.80 / 3.05 / 3.30 mm

The following figure shows design of the SoC cover.

WW.YYYY – packaging date: week number, year

T1 K1925BM018 – part number:

- before 2019 part number is T1 K1925BM018
- from 2019 part number is BE-T1000, as described in 7 Ordering Information

Figure 6-1 BE-T1000 package marking

The sketch diagram of the BE-T1000 package is shown in the following figure.

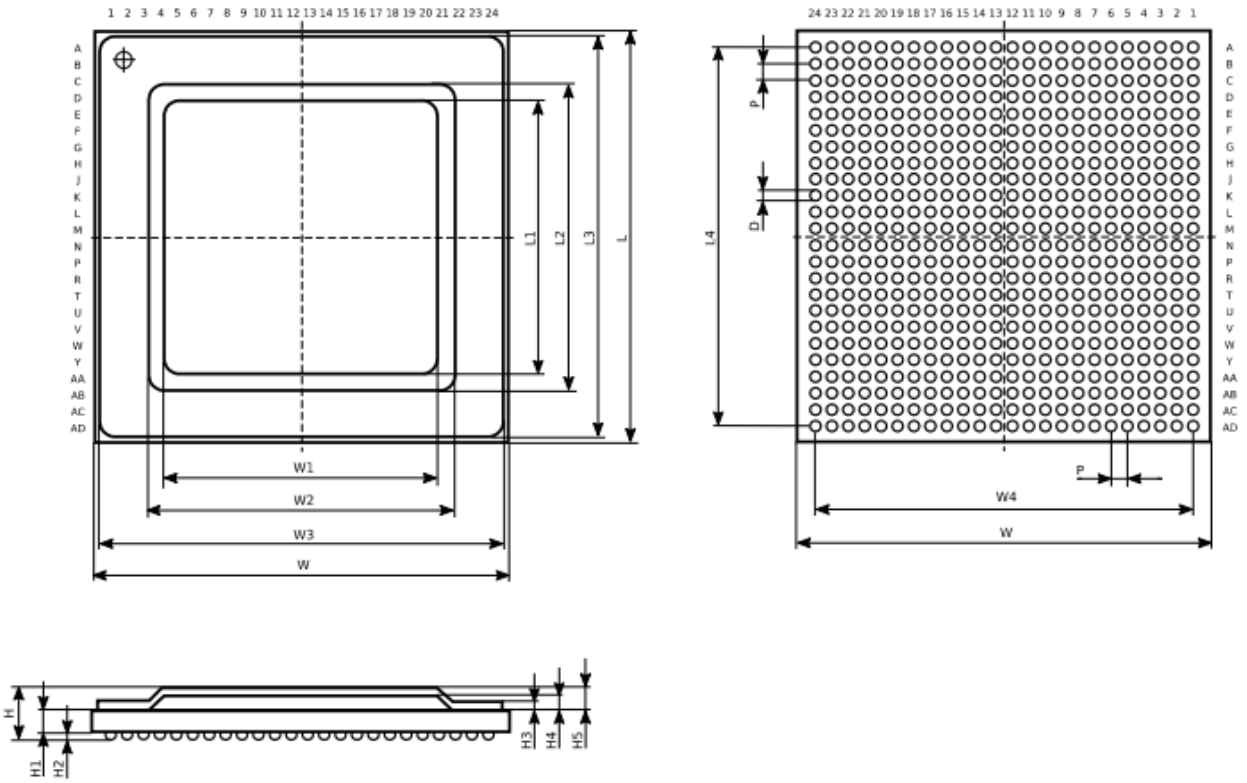

Figure 6-2 BE-T1000 Package Overview

The dimensions indicated in the diagram above are listed in the following table.

Table 6-2 BE-T1000 Package Dimensions

Notation	Dimensions (mm)	Note
L	25.0	Package length
L1	16.60±0.05	
L2	18.60	
L3	24.60±0.15	
L4	23.0	Edge ball center to center
W	25.0	Package width
W1	16.60±0.05	
W2	18.60	
W3	24.60±0.15	
W4	23.0	
H	2.8-3.3	Total package thickness including balls. Median value: 3.05 mm

Table 6-2 BE-T1000 Package Dimensions (continued)

Notation	Dimensions (mm)	Note
H1	1.15±0.15	Substrate thickness
H2	0.4–0.6	Stand off
H3	0.50±0.05	Heat spreader thickness
H4	0.80±0.05	
H5	1.30±0.05	
D	0.6±0.1	Ball diameter
P	1.0	Pitch

6.2 Packing

The processors are shipped in trays, 44 pieces per tray. A sketch diagram of the tray is shown in the following figure.

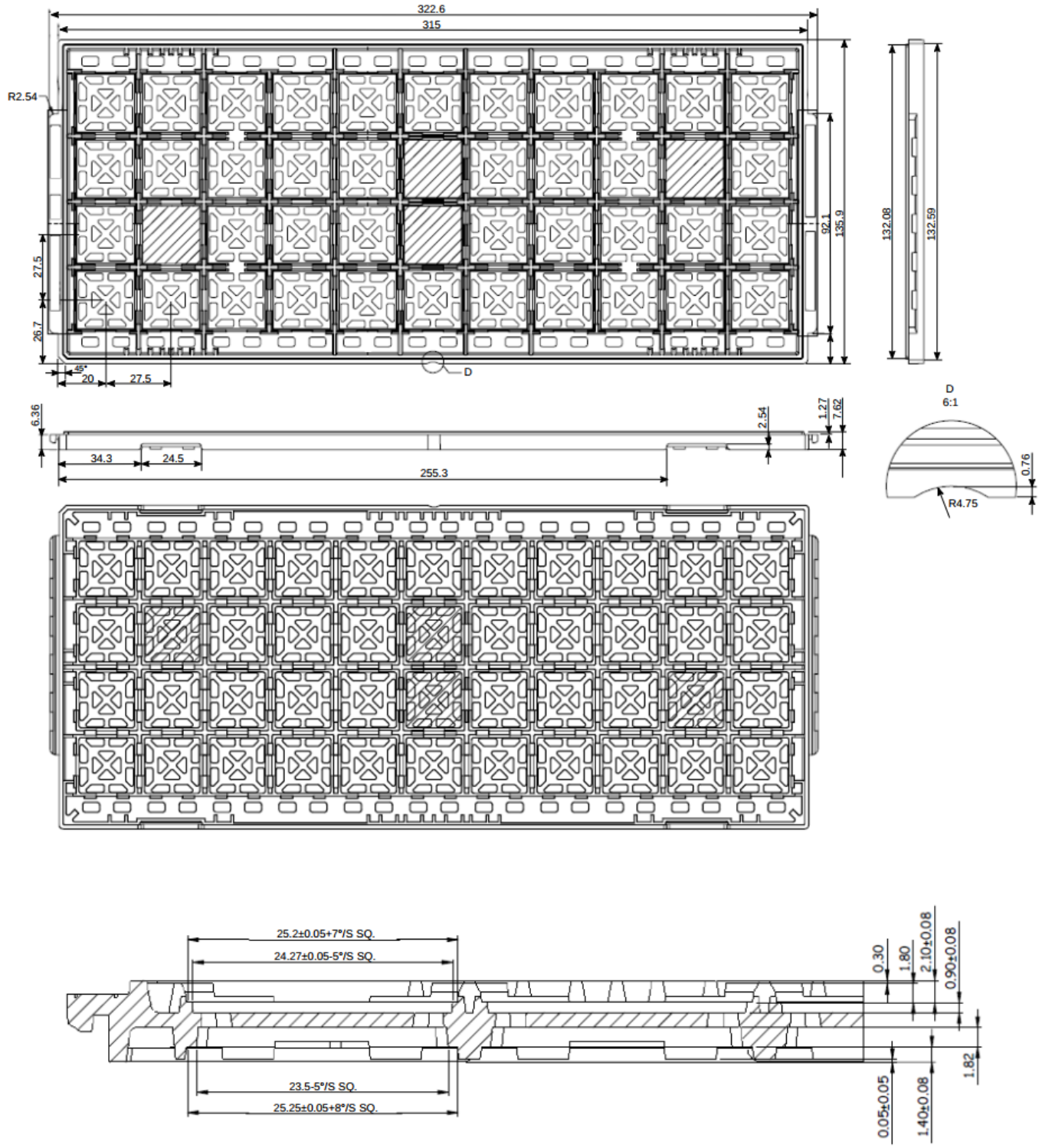

Figure 6-3 BE-T1000 Packing Tray Overview

6.3 Soldering Profile

The temperature profile recommended for mounting the BE-T1000 chip is provided in the following table.

Table 6-3 Recommended Soldering Profile for BE-T1000

Temperature	Time
RT to 140°C	60–90 sec
140°C to 180°C	60–120 sec
Time above 183°C	60–150 sec
Peak temperature	220°C ± 5°C
Time within 5°C peak temperature	10–20 sec
Ramp-down rate	6°C/sec maximum

The relevant graph is shown in the following figure.

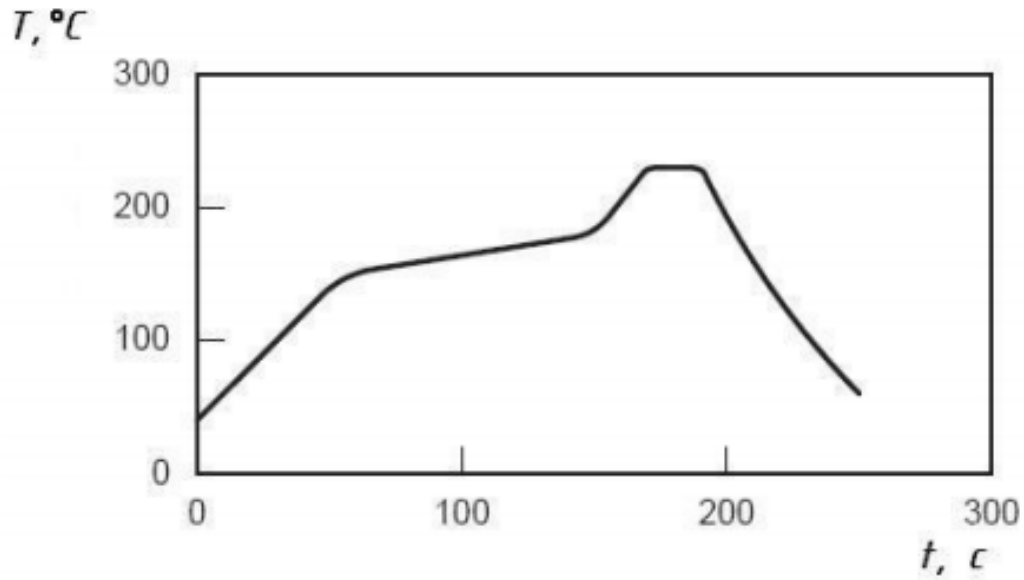

Figure 6-4 BE-T1000 Soldering Profile

7 Ordering Information

BE-T1000 is orderable part number. Designation of each field in the part number is shown in a table below.

Table 7-1 Part Number Structure

BE	-	T	1	0	0	0
Baikal Electronics	field delimiter	product line	generation	modification	reserved field	packaging

BE-T1000 is the first product in BE-T product line.

To order BE-T1000 please contact Baikal Electronics Company referred in the next chapter.

Contact Info

Baikal Electronics: https://www.baikalelectronics.com/

Head Office: https://www.baikalelectronics.com/contacts/

Mail: info@baikalelectronics.ru

Phone: +7 495 221-39-47

Revision History

Revision	Date	Substantive change(s)
1.0	Feb. 3, 2016	Identical to the public release, version 1.0 dated December 10, 2015, in English
2.0	Aug. 17, 2016	Power domains and PIN-out description; package dimensional drawing updated. Processor start and reset sequence added.
2.1	Sep. 16, 2016	Sections 6.3 Packaging and 6.4 Soldering Profile added in accordance with a release 2.0 dated September 12, 2016 in English
2.2	Feb. 17, 2017	Power domains frequency and voltage updated
2.3	Oct. 11, 2018	Added design of processor cover of the Baikal-T1
2.5	Apr. 22, 2019	Corrections of document title and formatting Corrections of block diagram Ordering info is added Info about TC1 test samples is removed Chapters 1 and 2 are updated
2.60	June 5, 2019	Chapter 5 Pin Assignment is updated
3.03	July 1, 2019	Terminology and formatting corrections
3.04	Dec. 10, 2019	Chapter 4 Processor Start and Reset is updated
3.05	Dec. 18, 2019	Minor edits
3.06	May 15, 2020	Minor edits