BE-M1000 Microprocessor
Datasheet

Document ID: BE-M1-DS-Eng#1204

1 Introduction

The BE-M1000 is a general purpose *System-on-a-Chip* (**SoC**) for computing systems, such as personal computers, microservers, networking equipment, multimedia and software-defined hardware, embedded systems and controllers that require high performance and low power consumption.

The SoC features eight Arm® Cortex™-A57 cores that operate at 1.5 GHz and support the coherent caches L1, L2, and L3.

The video subsystem includes two video controllers (LVDS and HDMI), and HD video decoder. Arm Mali™-T628 graphics coprocessor contains eight shader cores.

The SoC contains two DDR3/4 memory controllers and a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 3.0, USB 2.0, SATA 6G, eMMC/SD, I^{2}S, SPI, UART, I^{2}C, GPIO, etc.

The SoC complies with [Arm TrustZone® technology](#) and capabilities necessary to build trusted systems are included.

1.1　Main Features

Table 1-1 Main features

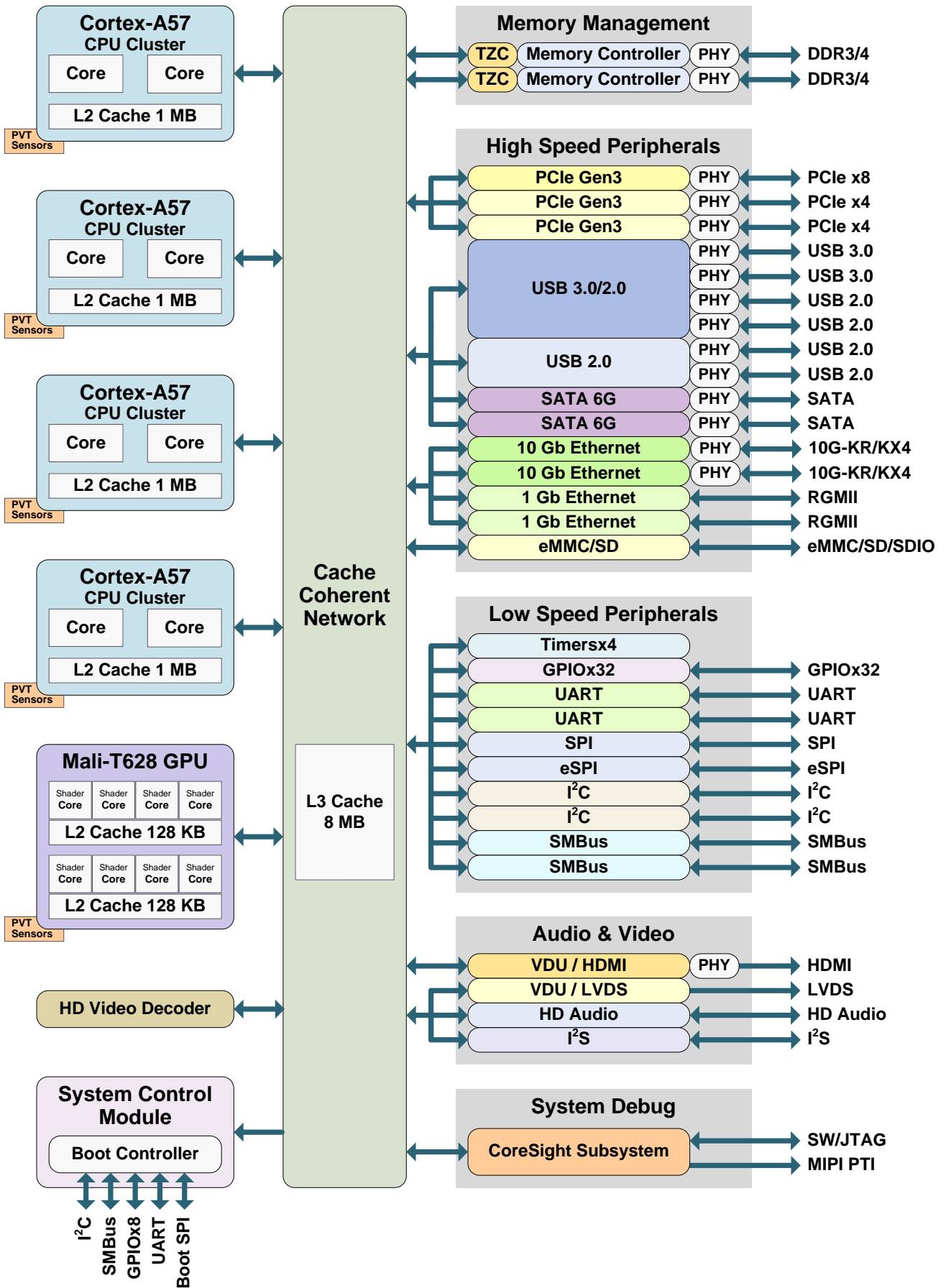| Feature	Description
Armv8-A Architecture	8 Arm Cortex-A57 cores operating at up to 1.5 GHz
	4 core clusters (2 cores and 1 MB L2 cache per cluster)
Graphics Processing Unit	Arm Mali-T628 *Graphics Processing Unit* (**GPU**) with 8 shader cores (two quad-core clusters) operating at 750 MHz
	128 KB L2 cache in a cluster
L3 Cache	*Cache Coherent Network* (**CCN**) with 8 MB L3 cache memory
External Memory Interface	Two 64-bit *Dynamic Random Access Memory* (**DRAM**) interfaces with support of DDR4-2400/DDR3-1600 and *Error Correction Code* (**ECC**)
	Up to 128 GB (up to 64 GB per channel)
High Speed Peripheral Interfaces	Three PCIe Gen3 interfaces: one PCIe x8 and two PCIe x4
	Two USB 3.0/2.0 ports and four USB 2.0 ports
	Two SATA 6G subsystems
	Two 10 Gb Ethernet interfaces (10GBASE-KX4/10GBASE-KR)
	Two 1 Gb Ethernet RGMII
	eMMC/SD/SDIO
Low Speed Peripheral Interfaces	Four peripheral timers
	32 independent GPIO lines
	Two UARTs
	SPI
	eSPI
	Two I^{2}Cs
	Two SMBus interfaces
Multimedia	Independent video controller with LVDS interface
	Independent video controller with HDMI 2.0
	HD video decoder
	HD audio controller
	I^{2}S interface
Security	Arm TrustZone architecture
	Two TrustZone controllers
	Hardware support for secure boot
System Monitoring and Debug	Five PVT sensor blocks
	Arm CoreSight™ debug and trace architecture
Package	FCBGA-1521 40x40 mm, 1 mm pitch, 1521 pins
Power Consumption	35 W max
Operating Temperature	From 0 to +70°C
Technology	CMOS 28 nm

1.2   Block Diagram

Figure 1-1 Block diagram

2 Detailed Description

2.1 Arm Cortex-A57 Clusters

The SoC contains 8 Arm Cortex-A57 cores in 4 clusters.

The Cortex-A57 cluster is a high-performance, low-power device that implements the Armv8-A architecture.

Each cluster contains two cores (up to 1.5 GHz) and L2 (1 MB) cache.

Each core contains 48 KB L1 instruction cache and 32 KB L1 data cache.

None of the cores in the clusters include optional Arm Cortex-A57 core Cryptographic Engine.

A core can operate in one of two possible states: secure and non-secure. By propagating the security state of the core through the on-chip interconnect to target-based transaction filters, the TrustZone technology is extended through the SoC architecture, creating a robust platform supporting fully isolated trusted and non-trusted worlds.

2.2 Memory Management

2.2.1 DDR3/4 Memory Subsystem

The SoC supports two memory channels. Each channel contains TrustZone controller, DDR controller and DDR PHY.

Each subsystem supports the following features:

- Up to 64 GB physical memory per channel

- Up to 4 memory ranks per channel

- Integrated PHY

- Integrated TrustZone controller to provide capabilities for building trusted systems

- 64/32-bit DDR3 (speed grades up to DDR3-1600)

- 64/32-bit DDR4 (speed grades up to DDR4-2400)

- ECC: *Single Error Correction*/*Double Error Detection* (**SEC**/**DED**)

- 1:2 frequency ratio mode

- Software power management support

- Programmable support for 1T/2T memory command timing

- Software programmable *Quality of Service* (**QoS**)

- Automatic DDR3/4 low power mode operation

2.2.2 DMA Controller for Low Speed Peripherals

The *DMA Controller* (**DMAC**) for Low Speed Peripherals implements capability of direct data transfer between a low speed device that is connected to a low speed peripheral and memory without CPU usage.

It allows to increase system performance by decreasing a load of the SoC cores.

The DMAC can only work in non-secure mode and supports the following features:

- Handshaking interfaces with two UARTs, SPI, and two I^{2}C controllers

- Eight unidirectional channels

- Multi-block transfers

- Single FIFO per channel for each source and destination

- Automatic data packing or unpacking to configure FIFO width

2.3   Cache Coherent Network

The CCN is based on the Arm CoreLink™ CCN-504 and interconnects the main SoC subsystems and manages the Level 3 cache for these subsystems.

The CCN provides the following key features:

- Dual simplex ring-bus interconnect topology

- Broadcast snoop channel

- DVM message transport between masters

- QoS regulation for shaping traffic profiles

- Performance-related events monitoring

- Error signal gathering using an error bus, with a combined interrupt to interrupt controller

- Separate caches for secure and non-secure transactions

2.4   System Control Module

System control module is used to manage all SoC subsystems.

It contains the following main blocks:

- *System Control Processor* (**SCP**) that runs service functions such as:

    o   Starts the SoC

    o   Provides the initial configuration of all the SoC modules

    o   Monitors the state of the SoC

- *Clock Management Unit* (**CMU**) that controls system clock and reset signals

- Boot controller that contains dedicated SPI used for initial boot

- UART, SMBus, GPIOx8, and I^{2}C controllers used for system control functions

    NOTE: These interfaces are under SCP control and are not available for Arm Cortex A-57 cores. The interfaces can be used if they have special support from the SDK.

2.5   High Speed Peripherals

2.5.1   PCIe Gen 3.0

The SoC contains three *PCI Express* (**PCIe**) interfaces:

- PCIe x8 with 64 GT/s transfer rate

- Two PCIe x4, each with 32 GT/s transfer rate

Each PCIe interface contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the **PCI Express Base Specification 3.0**.

Each PCIe provides the following main features:

- Integrated PHY

- Transfer rates up to 8.0 GT/s (~1GB/s) per single lane

- PCIe *Active State Power Management* (**ASPM**)

- PCIe *Advanced Error Reporting* (**AER**) with multiple header logging

- *Internal Address Translation Unit* (**iATU**)

- Embedded DMA controller with four write channels and four read channels

- Automatic lane reversal

- ECRC generation and checking

- Maximum payload size:

    o 256 bytes for PCIe x4

    o 512 bytes for PCIe x8

- One virtual channel for PCIe x4, two virtual channels for PCIe x8

Each PCIe controller can work either in secure or non-secure modes.

2.5.2 USB 3.0/2.0

The SoC contains two *Universal Serial Bus* (**USB**) controllers (USB 3.0/2.0 and USB 2.0) and six integrated PHY that provide six interfaces: two USB 3.0 interfaces and four USB 2.0 interfaces.

The USB 3.0/2.0 controller is compatible with the ***xHCI Specification*** by Intel Corporation. The controller is optimized for the Super-Speed applications and systems and supports the following device types:

- Super-Speed devices via USB 3.0 interface (4 Gbps IN and 4 Gbps OUT)

- High-Speed, Full-Speed, and Low-Speed devices via any interface

Each USB 3.0/2.0 interface work either in secure or non-secure mode.

The USB 2.0 controller is compatible with the ***xHCI Specification*** by Intel Corporation. It is optimized for the high-bandwidth applications and systems and supports the following device types:

- High-Speed (480 Mbps)

- Full-Speed (12 Mbps)

- Low-Speed (1.5 Mbps)

Each USB 2.0 interface can work either in secure or non-secure modes.

2.5.3 SATA 6G

The SoC contains two identical *Serial ATA* (**SATA**) subsystems. Each SATA is compliant with ***Serial ATA 3.2*** and ***AHCI Revision 1.3*** specifications and supports the following features:

- Integrated PHY

- SATA 6.0 Gb/s speeds

- 8b/10b encoding/decoding

- Error correction code

- Power management features including automatic partial-to-slumber transition

- Embedded DMA controller with transmit and receive channels

Each SATA can work either in secure or non-secure modes.

2.5.4 10 Gb Ethernet

The SoC contains two identical 10 Gb Ethernet interfaces, which enable to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gbps Ethernet: 10GBASE-KX4 and 10GBASE-KR.

Each interface contains a *10 Gb Ethernet Media Access Controller* (**XGMAC**) with integrated *10 Gigabit Ethernet Physical Coding Sublayer* (**XPCS**) and 10 Gb Ethernet PHY. Each XGMAC is fully compliant with clause 78 (*Energy Efficient Ethernet* (**EEE**) feature) of the IEEE 802.3az, standard for 10 Gbps operation.

Each XGMAC supports the following main features:

- Full-duplex mode at 10 Gbps

- Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard

- Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames

- Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard

- Embedded DMA controller with eight write channels and eight read channels

Each XGMAC can work either in secure or non-secure modes.

2.5.5 1 Gb Ethernet

The SoC contains two identical *1 Gigabit Media Access Controllers* (further **GMAC**).

Each GMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

Each GMAC supports the following main features:

- 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY

- Full-duplex and half-duplex modes are supported

- Embedded DMA controller with transmit and receive channels

Each GMAC can work either in secure or non-secure modes.

2.5.6 eMMC/SD

Embedded Multimedia Card (**eMMC**)/*Secure Digital* (**SD**) controller provides communication with memory cards and is compatible with the ***SD UHS-I*** and ***eMMC*** specifications. SD memory and *Secure Data Input/Output* (**SDIO**) digital interface protocol are compliant with ***SD HCI Specification***. The eMMC supports ***eMMC 5.1 protocol***.

The eMMC/SD controller supports the following features:

- SD-HCI host version 4 mode or less

- Embedded DMA controller

- Software tuning in SD UHS-I and eMMC modes

2.6 Low Speed Peripherals

2.6.1 GPIOx32

The *General Purpose Input/Output* (**GPIO**) provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

The GPIO contains 32 individually controllable signals in a single port. It implements run-time 32-bit programmable interface for external communications.

2.6.2 UART

There are two identical *Universal Asynchronous Receiver-Transmitters* (**UART**) in the SoC.

Each UART contains a handshaking interface with the DMA Controller for Low Speed Peripherals that can request and control non-secure data transfers between the UART and memory.

Each UART contains registers that control:

- Programmable character properties, such as:
    - Number of data bits per character (5-8)
    - Optional parity bit (with odd, even select or stick parity)
    - Number of stop bits (1, 1.5 or 2) Baud rates up to 1.5 Mbaud
- Parity generation/checking
- Interrupt generation

The voltage levels of the UART signals are shown in the following table.

Table 2-1 Voltage levels of the UART signals

Voltage level	Voltage, V
Low level ("0")	0÷0.45
High level ("1")	1.17÷1.8

2.6.3 SPI

The *Serial Peripheral Interface* (**SPI**) is a full-duplex serial master interface that supports Motorola SPI protocol. It provides short distance communication with up to four external slave SPI devices (SSx4).

The SPI controller supports the following features:

- Programmable delay on the sample time of the received serial data bit
- Dynamic control of the serial bit rate of the data transfer
- Programmable transfer data item size (4 to 16 bits)

It contains a handshaking interface with the DMA Controller for Low Speed Peripherals that can request and control data transfers between the SPI and memory.

2.6.4 eSPI

The *Enhanced Serial Peripheral Interface* (**eSPI**) is a synchronous serial communication interface used for short distance communication with up to eight external slave devices (SSx8).

Additional eSPI signals in comparison with SPI Interface:

- `RESET` programmable as input or output

- `ALERT` input interrupts

An eSPI device communicates in full-duplex mode using master-slave architecture with up to eight external slave SPI devices (SSx8). It supports single/dual/quad SPI mode of operation.

2.6.5 I^2C

There are two identical general purpose *Inter-Integrated Circuit* (I^2C) controllers in the SoC.

The I^2C controller provides support for the communications link between the devices connected to the bus.

Each I^2C controller supports the following features:

- Three modes:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
  - High-speed mode (≤ 3.4 Mb/s)
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers

Each I^2C controller uses handshaking interface with the [DMA Controller for Low Speed Peripherals](#) that can request and control non-secure data transfers between the I^2C and memory.

2.6.6 SMBus

The SoC includes two identical *System Management Bus* (**SMBus**) interfaces.

This interface provides a two-wire bidirectional interface for transfer of bytes of information between multiple compliant I^2C devices, typically with a microprocessor behind the DB-I^2C master/slave controller and one or more master/slave devices.

2.7   Audio & Video

2.7.1 Arm Mali-T628 GPU

This *Graphic Processin Unit* (**GPU**) a complete graphics acceleration platform based on open standards. It supports 2D graphics, 3D graphics, and *General Purpose Computing on GPU* (**GPGPU**).

The graphics processor provides the following elements:

- Two clusters
- Four shader cores operating at 750 MHz per each cluster
- 128KB L2 cache per each cluster

The graphics processor provides the following main features:

- Seamless load balancing across active shader cores

- The following APIs are supported:
    - o OpenGL ES 1.1, 2.0, 3.0, 3.1
    - o OpenCL 1.1
    - o RenderScript

- *Full Scene Anti-Aliasing* (4x**FSAA**, 16x**FSAA**) with minimal performance drop

- *Adaptive Scalable Texture Compression* (**ASTC**): *Low Dynamic Range* (**LDR**) and *High Dynamic Range* (**HDR**) are supported

- Native hardware support for 64-bit scalar and vector, integer and floating-point data

It can work both in secure and non-secure modes.

2.7.2   HD Video Decoder

High Definition (**HD**) Video Decoder is used:

- H.265 (HEVC)

- H.264, MPEG4, MPEG2, VP8, VP6, VC1, AVS, RealVideo, and JPEG: up to 1080p at 60 fps

The decoder loads encoded video data from the system memory, decodes it and places the information ready to be sent to the video display unit into the frame buffer.

It can work either in secure or non-secure modes.

2.7.3   VDU with Quad LVDS

Visual Display Unit (**VDU**) with quad *Low-Voltage Differential Signaling* (**LVDS**) is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

The module provides the following main features:

- Display resolution up to 2560x1440 pixels

- Color resolution of up to 24 bpp

- Embedded DMA controller

- Programmable vertical and horizontal timing parameters

2.7.4   VDU with HDMI 2.0

The VDU with *High Definition Multimedia Interface* (**HDMI**) provides a complete HDMI interface for transmitting video and audio data to an HDMI-compliant device, such as a computer monitor, video projector, digital television, or digital audio device.

The subsystem supports the following main features:

- Display resolution up to 2560x1440 pixels

- Color resolution of up to 24 bpp

- Embedded DMA controller

- Programmable vertical and horizontal timing parameters

- Three TMDS data channels with 6 Gbps data rate per channel

- Total maximum throughput of up to 18 Gbps (6 Gbps * 3 channels)

- HDMI 2.0 specification features:
    - All CEA-861-F video formats
    - *Dynamic Range and Mastering Infoframe* (**DRM**)
- Audio stream bit rate up to 24.576 Mbps
- It can work both in secure and non-secure modes

2.7.5 HD Audio

The HD Audio controller operates with multiple input and output audio channels and interacts with external high definition audio devices. It contains DMA engines, each of which can be set up to transfer a single audio "stream" to memory from the codec or from memory to the codec depending on the DMA type.

The HD audio controller supports the following features:

- Up to four input streams
- Up to four output streams
- Two serial data outputs (SDO 0 and SDO 1 are outputs to the codecs)
- Two serial data inputs (SDI 0 and SDI 1 are inputs from the codecs)
- Up to 192 kHz sample rate
- Up to 32 bit width per stream
- Number of channels: 10 (7.1 surround sound + 2)
- Four SDO DMA engines
- Four SDI DMA engines

  NOTE: The HD Audio controller supports only sample base rate of 48 kHz with a divider (2..8) and multiplier (2..4) for this base rate.

To support another sampling rate, for example, 44.1 or 11.025 kHz, you have to provide software resampling.

2.7.6 I^2S

The *Inter-IC Sound* (**I²S**) is a programmable module used for the serial communication with peripherals.

It is designed to be used in systems that process digital audio signals, such as:

- A/D and D/A converters
- Digital signal processors
- Error correction for compact disc and digital recording
- Digital filters
- Digital input/output interfaces

2.8   System Monitoring and Debug

2.8.1 PVT Controllers

The SoC contains five *Process, Voltage and Temperature* (**PVT**) sensor blocks used to monitor PVT in the Cortex-A57 clusters and Mali-T628 GPU.

2.8.2 CoreSight Subsystem

The CoreSight subsystem provides a standard implementation of the Arm Debug Interface for debug tools to work with:

- Serial Wire or JTAG Debug Port

- Trace Port Interface

The subsystem supports the following methods of debugging the SoC:

- "External" debug – conventional debug through the SW/JTAG interface

- "Self-hosted" debug – conventional debug with the processor running using a debug monitor that resides in memory

- Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the *Trace Port Interface* (**MIPI PTI**) to an external debug system

It can work either in secure or non-secure modes.

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification.

3.1 Power Supply Parameters

BE-M1000 requires six voltage supplies and single unified ground supply as shown in the following table.

Table 3-1 BE-M1000 power domains

Supply type	Package pin name	Voltage, V	Max power, W
Core supply	VDD		
0.95V voltage supply	VDD_HDMI_09 VDD_USB2_09 VDD_USB3_0_09 VDD_USB3_1_09 VDD_USB3TX_0_09 VDD_USB3TX_1_09 VDD_USB3_VP_0_09 VDD_USB3_VP_1_09 VDD_PCIE4_0_09 VDD_PCIE4_1_09 VDD_PCIE8_09 VDD_SATA_09 VDD_SATATX_09 VDD_XG0_09 VDD_XG1_09	$0.95 \pm 5\%$	24
PLL supply	VDDPLL_0_09 VDDPLL_1_09 VDDPLL_2_09 VDDPLL_3_09 VDDPLL_HDMI_09	$0.95 \pm 5\%$	0.20
DDR supply	VDDQ_DDR0 VDDQ_DDR1	$1.2 \pm 5\%$	6.0
1.5V voltage supply	VDD_PCIE4_0_15 VDD_PCIE4_1_15 VDD_PCIE8_15 VDD_XG0_15 VDD_XG1_15	$1.5 \pm 5\%$	2.0

Supply type	Package pin name	Voltage, V	Max power, W
1.8V voltage supply	VDD_DDR0_PLL VDD_DDR1_PLL VDD_HDMI_18 VDD_PVT_18 VDD_SATA_18 VDD_USB2_18 VDDIO_18 VDD_FUSE_18	1.8 ± 10%	1.8
3.3V voltage supply	VDD_SD_33 VDD_USB2_0_33 VDD_USB2_1_33 VDD_USB2_2_33 VDD_USB2_3_33 VDD_USB3_33	3.3 -6.9% +4.8%	0.7
Ground	VSS	0 ± 5%	0
Total			**~34.7W**

For more information, see Power Supply Requirements.

3.2   External Clocking

3.2.1 Reference Clock Signals

Table 3-2 Reference clock signals

Clock signal	Pin names	Frequency	Notes
Reference clock	CLK25M	25 MHz	
XGbE PHY reference clock	XG0_REF_CLKN[1,2] XG0_REF_CLKP[1,2] XG1_REF_CLKN[1,2] XG1_REF_CLKP[1,2]	156.25 MHz	Differential pair Terminated[4] and unterminated[5] clocks
PCIe PHY reference clock	PCIE4_0_REF_CLKN[1,2] PCIE4_0_REF_CLKP[1,2] PCIE4_1_REF_CLKN[1,2] PCIE4_1_REF_CLKP[1,2] PCIE8_REF_CLKN[1,2] PCIE8_REF_CLKP[1,2]	100 MHz	
SATA PHY reference clock	SATA_REFCLKP[1,2] SATA_REFCLKM[1,2]	100 MHz	

Clock signal	Pin names	Frequency	Notes
USB 3.0 PHY reference clock input	USB3_0_REFCLKN[3] USB3_0_REFCLKP[3] USB3_1_REFCLKN[3] USB3_1_REFCLKP[3]	100 MHz	Differential pair
USB 2.0 PHY: XI - crystal oscillator XO - crystal oscillator or board reference clock input	USB2_0_XI[1,2] USB2_0_XO[1,2] USB2_1_XI[1,2] USB2_1_XO[1,2] USB2_2_XI[1,2] USB2_2_XO[1,2] USB2_3_XI[1,2] USB2_3_XO[1,2]	50 MHz	
HDMI PLL reference clock input	HDMI_PLL_27M[1,2]	27 MHz	
LVDS PLL reference clock input	LVDS_PLL_27M[1,2]	27 MHz	

NOTE:

1   If the reference clock pins are unused, they should be tied off to the ground potential.

2   Reference clocks connect as needed.

3   When one USB 3.0 port is used, a 100 MHz clock generator must be connected to the USB3_#_REFCLK pins. If both USB3.0 ports are not used, the USB3_#_REFCLK pins should be tied off to the ground potential.

4   With terminated clocks, a 50 Ohms termination resistor is soldered on the board close to the SoC, preventing clock reflections while providing a clock source to the PHY.

5   If the board clocks are unterminated, the clock's signal level will be doubled as it hits the high-impedance input of the PHY reference clock inputs. This effect can also be used to provide a clean clock to the PHY, but ensure that the signal swing of the reference clock is not too high after the amplitude being doubled.

3.2.2   Reference Clock Requirements

3.2.2.1   Reference Clock (CLK25M)

Table 3-3 Reference clock (CLK25M) requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable stand-by current			15	uA

3.2.2.2   SATA PHY Reference Clock

Table 3-4 SATA PHY reference clock requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Reference clock frequency offset	-350		350	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[1]
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

3.2.2.3   XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-5 XGbE PHY reference clock requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12 kHz to 20 MHz
Allowed jitter for 10GBASE-KX4			3.6	ps (rms)	Integrated from 12 kHz to 20 MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples

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[1]   VDREF_CLK/4 + VCMREF_CLK ≤ vp + diode forward-biasing voltage and VCMREF_CLK-VDREF_CLK/4 ≥ - diode forward biasing voltage

Parameter	Min	Typ	Max	Unit	Conditions
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.2.4   PCIe PHY Reference Clock

Table 3-6 PCIe PHY reference clock requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling

NOTE: 100 MHz is the only PCIe standard compliant frequency. When using a 125 MHz frequency, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter.

3.2.2.5   USB 3.0 PHY Reference Clock

The USB 3.0 PHY supports a wide range of input clock frequencies to support both host and device applications. The following table summarizes the requirements of the reference clock provided to the USB 3.0 PHY to support superspeed only or both superspeed and high-speed operations.

Table 3-7 USB 3.0 PHY reference clock requirements

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency		100		MHz	
Reference clock frequency stability	-300		300	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock skew			200	ps	
Reference clock cycle-to-cycle jitter			150	ps	DJ over all frequency
Duty cycle	40		60	%	
Common mode input level	0		1.32	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[1]

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[1] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward biasing voltage and VCMREF_CLK – VDREF_CLK / 4 ≥ –diode forward biasing voltage

Parameter	Min	Typ	Max	Unit	Conditions
Single-ended input logic: Low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic: High	vp-0.3		vp	V	If single-ended input is used
Input edge rate	0.6		4	V/ns	
Required external reference resistance		200		Ohms	± 1% accuracy

3.2.2.6   USB 2.0 PHY Reference Clock

The USB 2.0 PHY supports the following reference clock sources:

- **Crystal Oscillator connected to the USB2_*_XI and USB2_*_XO pins**: The crystal oscillator must have a frequency tolerance of ±400 ppm, peak jitter of ±100 ps, and an output differential voltage of no less than 500 mV with respect to the XI signal

- **External Clock connected to the USB2_*_XO pin**: The clock must have a fundamental frequency of 50 MHz, with a frequency tolerance of ± 400 ppm, peak jitter of ± 100 ps, duty cycle between 40/60 and 60/40 percent, and signal swing of 1.8V.

3.2.2.7   HDMI PLL Reference Clock

Table 3-8 HDMI PLL reference clock requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

3.2.2.8   LVDS PLL Reference Clock

Table 3-9 LVDS PLL reference clock requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

4 Power-Up/Down

4.1 Power-Up Sequence

The following steps have to be performed to power up the SoC:

1. Provide the RESET_N reset signal (active is low)

2. Apply voltages to power pins according to [Power Supply Parameters](#) in the following order:

   - 3.3 V voltage supply

   - VDDPLL

   - VDDQ_DDR0

   - VDDQ_DDR1

   - 1.8 V voltage supply

   - Core supply and 0.95 V voltage supply

   - 1.5 V voltage supply

3. Provide the following reference clocks in the following order:

   - CLK25M

   - USB3_0_REFCLK

   - USB3_1_REFCLK

   - SATA_REFCLK

   - PCIE4_0_REF_CLK to CPU

   - PCIE4_1_REF_CLK and PCIE8_REF_CLK to CPU

   - PCIE4_0_REF_CLK, PCIE4_1_REF_CLK, PCIE8_REF_CLK to connector

4. Deassert the RESET_N signal

Once the RESET_N signal is deasserted, the boot controller provides initialization of clock and reset signals for each SoC subsystem, loads and executes the boot loader, which is stored in the boot SPI flash.

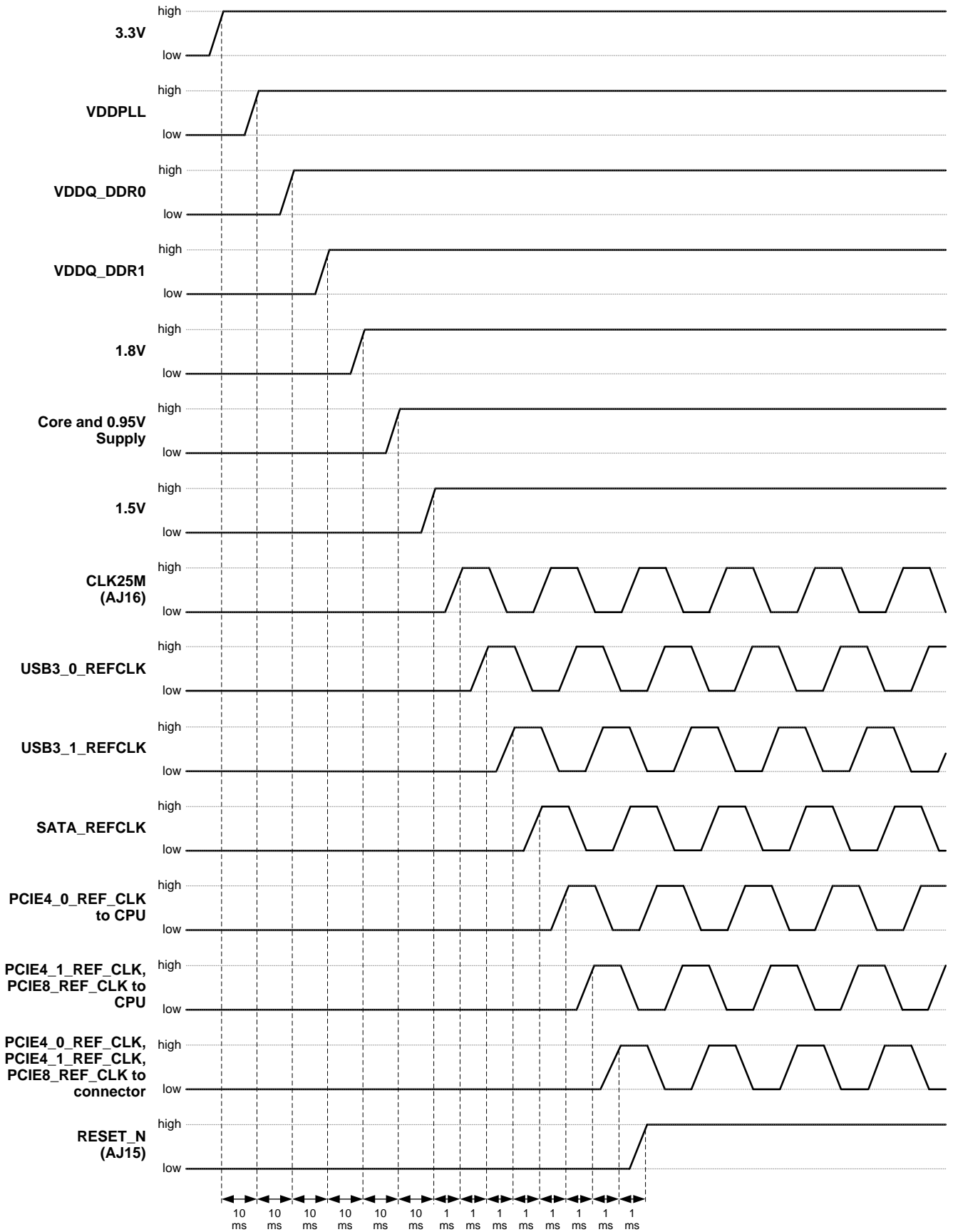The following figure shows start sequence for BE-M1000.

Figure 4-1 Start sequence diagram for the BE-M1000

NOTE: The time delays shown in the figure are recommended.

4.2   Power-Down Sequence

To power-down, turn off power supplies from power pins according to Power Supply Parameters in the following order:

- 1.5 V voltage supply

- Core supply and 0.95 V voltage supply

- 1.8 V voltage supply

- VDDQ_DDR1

- VDDQ_DDR0

- VDDPLL

- 3.3 V voltage supply

5 Pin Assignment

5.1   Pinout List

The following tables contain the list of I/O pins of the SoC including the power supply and ground pins. The following legend is applied for the following tables.

Legend:

I	Input
O	Output
IO	Input/Output
A	Analog
P	Power supply
G	Ground
NC	Not connected

NOTE: Pin IDs are represented in *BE-M1000 Pinout List*. The file is available in the description of BE-M1000 on Baikal Electronics website.

5.1.1 Memory Management

5.1.1.1 DDR3/4

Table 5-1 DDR pins

Pin name	Type	Description
DDR0_A[13:0]	O	SDRAM address
DDR0_A[14]	O	SDRAM WE
DDR0_A[15]	O	SDRAM CAS
DDR0_A[16]	O	SDRAM RAS
DDR0_A[17]	O	SDRAM A[17]
DDR0_ACT_N	O	When low, indicates the activate (open row) command
DDR0_ALERT_N	I	SDRAM CRC/parity error
DDR0_ATO	A	Analog test output (test pad) **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR0_BA[1:0]	O	SDRAM bank address
DDR0_BG[1:0]	O	SDRAM bank group
DDR0_CK[3:0]	O	SDRAM clock
DDR0_CK_N[3:0]	O	SDRAM clock
DDR0_CKE[3:0]	O	SDRAM clock enable
DDR0_CS_N[3:0]	O	SDRAM chip select
DDR0_DM[8:0]	IO	SDRAM data mask
DDR0_DQ[63:0]	IO	SDRAM data
DDR0_DQS[8:0]	IO	SDRAM data strobe
DDR0_DQS_N[8:0]	IO	SDRAM data strobe

Pin name	Type	Description
DDR0_DTO[1:0]	O	Digital test output (test pad) **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR0_ECC[7:0]	IO	SDRAM data ECC
DDR0_MIRROR	O	SDRAM mirror (optional DIMM signal)
DDR0_ODT[3:0]	O	SDRAM on-die termination
DDR0_PARITY	O	SDRAM parity
DDR0_QCSEN_N	O	SDRAM quad CS enable (optional DIMM signal)
DDR0_RAM_RST_N	O	SDRAM reset
DDR0_VREFI[9:0]	A	IO ring VREFI net **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR0_VREFI_ZQ	A	IO ring VREFI ZQ net
DDR0_ZQ	A	ZQ resistor (to external calibration resistor) Connects the pin through an external 240 ± 1% Ohms resistor to ground
DDR1_A[13:0]	O	SDRAM address
DDR1_A[14]	O	SDRAM WE
DDR1_A[15]	O	SDRAM CAS
DDR1_A[16]	O	SDRAM RAS
DDR1_A[17]	O	SDRAM A[17]
DDR1_ACT_N	O	When low, indicates the activate (open row) command
DDR1_ALERT_N	I	SDRAM CRC/parity error
DDR1_ATO	A	Analog test output (test pad) **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR1_BA[1:0]	O	SDRAM bank address
DDR1_BG[1:0]	O	SDRAM bank Group
DDR1_CK[3:0]	O	SDRAM clock
DDR1_CK_N[3:0]	O	SDRAM clock
DDR1_CKE[3:0]	O	SDRAM clock enable
DDR1_CS_N[3:0]	O	SDRAM chip select
DDR1_DM[8:0]	IO	SDRAM data mask
DDR1_DQ[63:0]	IO	SDRAM data
DDR1_DQS[8:0]	IO	SDRAM data strobe
DDR1_DQS_N[8:0]	IO	SDRAM data strobe
DDR1_DTO[1:0]	O	Digital test output (test pad) **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR1_ECC[7:0]	IO	SDRAM data ECC
DDR1_MIRROR	O	SDRAM mirror (optional DIMM signal)

Pin name	Type	Description
DDR1_ODT[3:0]	O	SDRAM on-die termination
DDR1_PARITY	O	SDRAM parity
DDR1_QCSEN_N	O	SDRAM quad CS enable (optional DIMM signal)
DDR1_RAM_RST_N	O	SDRAM reset
DDR1_VREFI[9:0]	A	IO ring VREFI net **NOTE:** Reserved in BE-M1000 manufactured since 2021.
DDR1_VREFI_ZQ	A	IO ring VREFI ZQ net
DDR1_ZQ	A	ZQ resistor (to external calibration resistor) Connects the pin through an external 240 ± 1% Ohms resistor to ground

5.1.2 High Speed Peripherals

5.1.2.1 PCIe x8

Table 5-2 PCIe x8 pins

Pin name	Type	Description
PCIE8_AMON0	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_AMON1	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_ATT_BUT	I	Indicates whether the system attention button is pressed **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_ATT_IND[1:0]	O	Controls the system attention indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_CMD_INT	I	Hot-plug controller command completed interrupt **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_DMON0	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_DMON1	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_DMONB0	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_DMONB1	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_INTRL_CTRL	O	Electromechanical Interlock Control **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_INTRL_ENG	I	System Electromechanical Interlock Engaged **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_MRL_SENS	I	*Manually-Operated Retention Latch* (**MRL**) sensor state Indicates the state of the MRL sensor: • 0: MRL is closed • 1: MRL is opened **NOTE:** Reserved in BE-M1000 manufactured since 2021.

Pin name	Type	Description
PCIE8_PRES_ST	I	Presence detect state **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_PWR_CTRL	O	Controls the system power controller **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_PWR_FAULT	I	Power fault detect **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_PWR_IND[1:0]	O	Controls the system power indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE8_RBIAS0	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
PCIE8_RBIAS1	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
PCIE8_REF_CLKN	I	Reference clock differential pair
PCIE8_REF_CLKP	I	Reference clock differential pair
PCIE8_RXN[7:0]	I	Receive data differential pair
PCIE8_RXP[7:0]	I	Receive data differential pair
PCIE8_TXN[7:0]	O	Transmit data differential pair
PCIE8_TXP[7:0]	O	Transmit data differential pair

5.1.2.2   PCIe x4

Table 5-3 PCIe x4 pins

Pin name	Type	Description
PCIE4_0_AMON	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_ATT_BUT	I	Indicates whether the system attention button is pressed **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_ATT_IND[1:0]	O	Controls the system attention indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_CMD_INT	I	Hot-plug controller command completed interrupt **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_DMON	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_DMONB	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_INTRL_CTRL	O	Electromechanical Interlock Control **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_INTRL_ENG	I	System Electromechanical Interlock Engaged **NOTE:** Reserved in BE-M1000 manufactured since 2021.

Pin name	Type	Description
PCIE4_0_MRL_SENS	I	MRL sensor state Indicates the state of the MRL sensor: • 0: MRL is closed • 1: MRL is opened **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_PRES_ST	I	Presence detect state **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_PWR_CTRL	O	Controls the system power controller **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_PWR_FAULT	I	Power fault detect **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_PWR_IND[1:0]	O	Controls the system power indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_0_RBIAS	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
PCIE4_0_REF_CLKN	I	Reference clock differential pair
PCIE4_0_REF_CLKP	I	Reference clock differential pair
PCIE4_0_RXN[3:0]	I	Receive data differential pair
PCIE4_0_RXP[3:0]	I	Receive data differential pair
PCIE4_0_TXN[3:0]	O	Transmit data differential pair
PCIE4_0_TXP[3:0]	O	Transmit data differential pair
PCIE4_1_AMON	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_ATT_BUT	I	Indicates whether the system attention button is pressed **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_ATT_IND[1:0]	O	Controls the system attention indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_CMD_INT	I	Hot-plug controller command completed interrupt **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_DMON	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_DMONB	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_INTRL_CTRL	O	Electromechanical Interlock Control **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_INTRL_ENG	I	System Electromechanical Interlock Engaged **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_MRL_SENS	I	MRL sensor state Indicates the state of the MRL sensor: • 0: MRL is closed • 1: MRL is opened **NOTE:** Reserved in BE-M1000 manufactured since 2021.

Pin name	Type	Description
PCIE4_1_PRES_ST	I	Presence detect state **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_PWR_CTRL	O	Controls the system power controller **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_PWR_FAULT	I	Power fault detect **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_PWR_IND[1:0]	O	Controls the system power indicator **NOTE:** Reserved in BE-M1000 manufactured since 2021.
PCIE4_1_RBIAS	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
PCIE4_1_REF_CLKN	I	Reference clock differential pair
PCIE4_1_REF_CLKP	I	Reference clock differential pair
PCIE4_1_RXN[3:0]	I	Receive data differential pair
PCIE4_1_RXP[3:0]	I	Receive data differential pair
PCIE4_1_TXN[3:0]	O	Transmit data differential pair
PCIE4_1_TXP[3:0]	O	Transmit data differential pair

5.1.2.3   USB 3.0/2.0

Table 5-4 USB 3.0/2.0 controller pins

Pin name	Type	Description
USB2_2_CTRL	O	Port power control
USB2_2_DM0	IO	USB D- signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, receives/transmits 3.3 V nominally
USB2_2_DP0	IO	USB D+ signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_2_ID0	IO	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY
USB2_2_OVCUR	I	Port overcurrent
USB2_2_RT	IO	Transmitter resistor tune Connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance
USB2_2_VBUS0	A	USB 5 V signal. This is the USB 5 V supply. A charge pump external to the USB 2.0 PHY must provide power to him. The nominal voltage is 5 V
USB2_2_XI	I	Crystal oscillator XI
USB2_2_XO	I	Crystal oscillator XO or board reference clock input **NOTE:** When the reference clock source is a crystal, XO is a connection to a crystal. When the reference clock source is an external board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input.

Pin name	Type	Description
USB2_3_CTRL	O	Port power control
USB2_3_DM0	IO	USB D- signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_3_DP0	IO	USB D+ signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_3_ID0	IO	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY
USB2_3_OVCUR	I	Port overcurrent
USB2_3_RT	IO	Transmitter resistor tune Connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance
USB2_3_VBUS0	A	USB 5 V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to him. The nominal voltage is 5 V
USB2_3_XI	I	Crystal oscillator XI
USB2_3_XO	I	Crystal oscillator XO or board reference clock input **NOTE:** When the reference clock source is a crystal, XO is a connection to a crystal. When the reference clock source is an external board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input.
USB2_4_CTRL	O	Port power control – USB 2.0 part
USB2_4_OVCUR	I	Port overcurrent – USB 2.0 part
USB2_5_CTRL	O	Port power control – USB 2.0 part
USB2_5_OVCUR	I	Port overcurrent – USB 2.0 part
USB3_0_CTRL	O	Port power control – USB 3.0 part
USB3_0_DM0	IO	USB 2.0 D- signal. In normal operation, it carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB3_0_DP0	IO	USB 2.0 D+ signal. In normal operation, it carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB3_0_ID0	IO	USB 2.0 mini-receptacle identifier
USB3_0_OVCUR	I	Port overcurrent – USB 3.0 part
USB3_0_REFCLKN	I	USB 3.0 reference clock input
USB3_0_REFCLKP	I	USB 3.0 reference clock input
USB3_0_RESREF	A	USB 3.0 external reference resistor Connects through a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board
USB3_0_RXON	I	USB 3.0 receive data

Pin name	Type	Description
USB3_0_RXOP	I	USB 3.0 receive data
USB3_0_TXON	O	USB 3.0 transmit data
USB3_0_TXOP	O	USB 3.0 transmit data
USB3_0_VBUS0	A	USB 5 V power supply. A charge pump external to the USB 3.0 PHY must provide power to him. The nominal voltage is 5 V
USB3_1_CTRL	O	Port power control – USB 3.0 part
USB3_1_DM0	IO	USB 2.0 D- signal. In normal operation, it carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB3_1_DP0	IO	USB 2.0 D+ signal. In normal operation, it carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB3_1_ID0	IO	USB 2.0 mini-receptacle identifier
USB3_1_OVCUR	I	Port overcurrent – USB 3.0 part
USB3_1_REFCLKN	I	USB 3.0 reference clock input
USB3_1_REFCLKP	I	USB 3.0 reference clock input
USB3_1_RESREF	A	USB 3.0 external reference resistor Connects through a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board
USB3_1_RXON	I	USB 3.0 receive data
USB3_1_RXOP	I	USB 3.0 receive data
USB3_1_TXON	O	USB 3.0 transmit data
USB3_1_TXOP	O	USB 3.0 transmit data
USB3_1_VBUS0	A	USB 5 V power supply. A charge pump external to the USB 3.0 PHY must provide power to him. The nominal voltage is 5 V

5.1.2.4 USB 2.0

Table 5-5 USB 2.0 controller pins

Pin name	Type	Description
USB2_0_CTRL	O	Port power control
USB2_0_DM0	IO	USB D- signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_0_DP0	IO	USB D+ signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_0_ID0	IO	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY
USB2_0_OVCUR	I	Port overcurrent

Pin name	Type	Description
USB2_0_RT	IO	Transmitter resistor tune Connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance
USB2_0_VBUS0	A	USB 5 V signal. This is the USB 5 V supply. A charge pump external to the USB 2.0 PHY must provide power to him. The nominal voltage is 5 V
USB2_0_XI	I	Crystal oscillator XI
USB2_0_XO	I	Crystal oscillator XO or board reference clock input **NOTE:** When the reference clock source is a crystal, XO is a connection to a crystal. When the reference clock source is an external board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input.
USB2_1_CTRL	O	Port power control
USB2_1_DM0	IO	USB D- signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_1_DP0	IO	USB D+ signal. In normal operation, it carries USB data to and from the USB 2.0 PHY. In HS operation, receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, receives/transmits 3.3 V nominally
USB2_1_ID0	IO	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY
USB2_1_OVCUR	I	Port overcurrent
USB2_1_RT	IO	Transmitter resistor tune Connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance
USB2_1_VBUS0	A	USB 5 V signal. This is the USB 5 V supply. A charge pump external to the USB 2.0 PHY must provide power to him. The nominal voltage is 5 V
USB2_1_XI	I	Crystal oscillator XI
USB2_1_XO	I	Crystal oscillator XO or board reference clock input **NOTE:** When the reference clock source is a crystal, XO is a connection to a crystal. When the reference clock source is an external board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input.

5.1.2.5 SATA

Table 5-6 SATA pins

Pin name	Type	Description
SATA_P0ACTLED	O	Port 0 activity LED Drives an external LED based on the port activity **Active state:** High
SATA_P0CPDET	I	Cold presence detect port 0 Detects addition or removal of the powered-down device
SATA_P0CPPOD	O	Cold presence power-on device port 0 Enables power to the external device when asserted

SATA_P0MPSW	I	Mechanical presence switch port 0 Indicates the state of the external device presence switch
SATA_P1ACTLED	O	Port 1 Activity LED Drives an external LED based on the port activity **Active state:** High
SATA_P1CPDET	I	Cold Presence Detect port 1 Detects addition or removal of the powered-down device
SATA_P1CPPOD	O	Cold Presence Power-On Device port 1 Enables power to the external device when asserted
SATA_P1MPSW	I	Mechanical Presence Switch port 1 Indicates the state of the external device presence switch
SATA_REFCLKM	I	Reference clock differential pair
SATA_REFCLKP	I	Reference clock differential pair
SATA_RESREF	A	Reference resistor Connect from a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board
SATA_RXN[1:0]	I	Receive data differential pair port 0 or port 1
SATA_RXP[1:0]	I	Receive data differential pair port 0 or port 1
SATA_TXN[1:0]	O	Transmit data differential pair port 0 or port 1
SATA_TXP[1:0]	O	Transmit data differential pair port 0 or port 1

5.1.2.6   10 Gb Ethernet

Table 5-7 XGbE pins

Pin name	Type	Description
XG0_AMON	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
XG0_DMON	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
XG0_DMONB	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
XG0_RBIAS	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
XG0_REF_CLKN	I	Differential reference clocks from pads
XG0_REF_CLKP	I	Differential reference clocks from pads
XG0_RXN[3:0]	I	Receive data differential pair
XG0_RXP[3:0]	I	Receive data differential pair
XG0_TXN[3:0]	O	Transmit data differential pair
XG0_TXP[3:0]	O	Transmit data differential pair
XG1_AMON	O	Analog monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.

Pin name	Type	Description
XG1_DMON	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
XG1_DMONB	O	Differential digital monitor bump **NOTE:** Reserved in BE-M1000 manufactured since 2021.
XG1_RBIAS	IO	Bias resistor bump Connects to 1 kOhms ± 1% precision resistor on board
XG1_REF_CLKN	I	Differential reference clocks from pads
XG1_REF_CLKP	I	Differential reference clocks from pads
XG1_RXN[3:0]	I	Receive data differential pair
XG1_RXP[3:0]	I	Receive data differential pair
XG1_TXN[3:0]	O	Transmit data differential pair
XG1_TXP[3:0]	O	Transmit data differential pair

5.1.2.7 1 Gb Ethernet

Table 5-8 GMAC pins

Pin name	Type	Description
G0_GP_IN	I	General purpose input
G0_GP_OUT	O	General purpose output
G0_MDC	O	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
G0_MDIO	IO	*Management Data Input/Output* (**MDIO**)
G0_RX_CLK	I	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G0_RX_DAT[3:0]	I	Receive data
G0_RX_DEN	I	Receive data
G0_TX_CLK	O	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G0_TX_DAT[3:0]	O	Transmit data
G0_TX_DEN	O	Transmit data enable
G1_GP_IN	I	General purpose input
G1_GP_OUT	O	General purpose output
G1_MDC	O	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
G1_MDIO	IO	*Management Data Input/Output* (**MDIO**)
G1_RX_CLK	I	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G1_RX_DAT[3:0]	I	Receive data
G1_RX_DEN	I	Receive data

Pin name	Type	Description
G1_TX_CLK	O	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G1_TX_DAT[3:0]	O	Transmit data
G1_TX_DEN	O	Transmit data enable

5.1.2.8 eMMC/SD

Table 5-9 eMMC/SD pins

Pin name	Type	Description
SD_CAP0	A	Connected to 1 uF capacitor for stabilizing LDO output voltage
SD_CAP1	A	Connected to 1 uF capacitor for stabilizing LDO output voltage
SD_CARD_DETECT_N	I	Card detect signal, active low. When this is 0, it indicates whether card is connected. When this signal goes from 0 to 1 card insertion interrupt is generated if enabled **NOTE:** This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device is non-removable, card detection is not required.
SD_CLK	O	SD card transmit/receive clock
SD_CMD	IO	SD card command
SD_DAT[7:0]	IO	SD card data **NOTE:** Input data line must be pulled high, even if it is not used.
SD_LED_CTRL	O	SD card LED control Warns user not to remove card while it is being accessed
SD_REG_VOL_STABLE	I	Check whether host regulator voltage is stable, active high
SD_RST_N	O	eMMC device reset, active low
SD_VDD_ON	O	Switch on VDD1/VDD bus power for SD/eMMC card
SD_VDD_SEL[0]	O	Select 1.8V voltage level for SD card
SD_VDD_SEL[1]	O	Select 3V voltage level for SD card
SD_VDD_SEL[2]	O	Select 3.3V voltage level for SD card
SD_WRITE_PROT	I	Card write protect, active high. When this is 1, it represents card is write protected **NOTE:** This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device does not have write protect physical switch similar to SD card, this signal is not required.

5.1.3 Low Speed Peripherals

5.1.3.1 GPIOx32

Table 5-10 GPIOx32 pins

Pin name	Type	Description
GPIO32[31:0]	IO	GPIO data

5.1.3.2 UART

Table 5-11 UART pins

Pin name	Type	Description
UART1_RXD	I	Receive data
UART1_TXD	O	Transmit data
UART2_RXD	I	Receive data
UART2_TXD	O	Transmit data

5.1.3.3 SPI

Table 5-12 SPI pins

Pin name	Type	Description
SPI1_CLK	O	Output clock
SPI1_RXD	I	Receive data
SPI1_SS_N[3:0]	O	Slave select
SPI1_TXD	O	Transmit data

5.1.3.4 eSPI

Table 5-13 eSPI pins

Pin name	Type	Description
ESPI_ALERT[7:0]	I	eSPI alert
ESPI_CLK	IO	eSPI clock
ESPI_DAT[3:0]	IO	eSPI data
ESPI_RST	IO	eSPI reset
ESPI_SS_N[7:0]	IO	eSPI slave select

5.1.3.5 I^2C

Table 5-14 I^2C bus pins

Pin name	Type	Description
I2C1_SCL	IO	I^2C #1 clock
I2C1_SDA	IO	I^2C #1 data
I2C2_SCL	IO	I^2C #2 clock
I2C2_SDA	IO	I^2C #2 data

5.1.3.6 SMBus

Table 5-15 SMBus pins

Pin name	Type	Description
SMB1_CLK	IO	SMBus #1 clock
SMB1_DAT	IO	SMBus #1 data

SMB2_CLK	IO	SMBus #2 clock
SMB2_DAT	IO	SMBus #2 data

5.1.4 Audio & Video

5.1.4.1 LVDS

Table 5-16 LVDS pins

Pin name	Type	Description
LED_PWM	O	Brightness control
LVDS_L0_CLKN	O	LVDS clock
LVDS_L0_CLKP	O	LVDS clock
LVDS_L0_DATN[3:0]	O	LVDS data
LVDS_L0_DATP[3:0]	O	LVDS data
LVDS_L1_CLKN	O	LVDS clock
LVDS_L1_CLKP	O	LVDS clock
LVDS_L1_DATN[3:0]	O	LVDS data
LVDS_L1_DATP[3:0]	O	LVDS data
LVDS_L2_CLKN	O	LVDS clock
LVDS_L2_CLKP	O	LVDS clock
LVDS_L2_DATN[3:0]	O	LVDS data
LVDS_L2_DATP[3:0]	O	LVDS data
LVDS_L3_CLKN	O	LVDS clock
LVDS_L3_CLKP	O	LVDS clock
LVDS_L3_DATN[3:0]	O	LVDS data
LVDS_L3_DATP[3:0]	O	LVDS data
LVDS_PLL_27M	I	PLL reference clock 27 MHz IN – LVDS
LVDS_VREF	A	Signal reference

5.1.4.2 HDMI

Table 5-17 HDMI pins

Pin name	Type	Description
HDMI_CLKN	O	Negative TMDS differential line driver clock output
HDMI_CLKP	O	Positive TMDS differential line driver clock output
HDMI_DATN[2:0]	O	TMDS data
HDMI_DATP[2:0]	O	TMDS data
HDMI_DB_BISTDONE	O	Indication of *Built-In Self Test* (**BIST**) test completion
HDMI_DB_BISTEN	I	Control enable signal for BIST test

Pin name	Type	Description
HDMI_DB_BISTOK	O	Indication of BIST test pass
HDMI_DB_DAT[9:0]	O	Indication that path between I/O pad and *Analog Front End* (**AFE**) is valid **NOTE:** Reserved in BE-M1000 manufactured since 2021.
HDMI_DB_EN	I	Control enable signal for I/O continuity test **NOTE:** Reserved in BE-M1000 manufactured since 2021.
HDMI_DB_ENHPDRXSENSE	I	Enables hot plug detect and RXSENSE for HDMI operation
HDMI_DB_EXTERNAL	I	HDMI PHY debug interface
HDMI_DB_PDDQ	I	Shuts off low-to-high bias voltage generators in the MPLL and support blocks, because the generators are not under direct power-down control
HDMI_DB_PHY_RESET	I	PHY reset. This signal places the digital section of the macro into a reset state
HDMI_DB_PHYDTB0	O	Digital test bus **NOTE:** Reserved in BE-M1000 manufactured since 2021.
HDMI_DB_PHYDTB1	O	Digital test bus **NOTE:** Reserved in BE-M1000 manufactured since 2021.
HDMI_DB_RXSENSE	O	Rx presence detection signal for all TMDS data lanes for HDMI mode of operation. Asserted high if TMDS lines have a 3.3V pull-up resistor connected to them
HDMI_DB_SNK_DET_I	O	Sink detected signal for HDMI **NOTE:** Reserved in BE-M1000 manufactured since 2021.
HDMI_DB_SVSRET_MODEZ	I	Enables retention mode
HDMI_DB_TX_PWRON	I	Power-on input. This signal is used to power up the entire macro. All analog blocks are released from power-down mode
HDMI_DB_TX_READY	O	Indicates that the HDMI PHY is ready to transmit data
HDMI_DDCCEC	IO	Ground reference for the hot plug detect signal
HDMI_HPD	IO	Hot plug detect signal for HDMI
HDMI_PLL_27M	I	PLL reference clock 27 MHz IN – HDMI
HDMI_RESREF	A	Reference resistor connection Connects to 1.62 ± 1% kOhms reference resistor (connected to ground)
HDMI_SCL	O	HDMI I^{2}C clock output
HDMI_SDA	IO	HDMI I^{2}C data

5.1.4.3 *HD Audio*

Table 5-18 HD audio pins

Pin name	Type	Description
HDA_BCLK	O	Codec link 24 MHz frequency **NOTE:** Reserved in BE-M1000 manufactured before 2021.
HDA_RST_N	O	Codec reset, active low **NOTE:** Reserved in BE-M1000 manufactured before 2021.
HDA_SDI[1:0]	IO	Codec serial data input **NOTE:** Reserved in BE-M1000 manufactured before 2021.

| HDA_SDO[1:0] | IO | Codec serial data output
NOTE: Reserved in BE-M1000 manufactured before 2021. |
| HDA_SYNC | O | Codec 48 kHz frame synchronization
NOTE: Reserved in BE-M1000 manufactured before 2021. |

5.1.4.4 I²S

Table 5-19 I²S pins

Pin name	Type	Description
I2S_SCK	I	I²S continuous serial clock
I2S_SDI	I	I²S serial data input
I2S_SDO	O	I²S serial data output
I2S_WS	I	I²S word select

5.1.5 System Control

Table 5-20 system control pins

Pin name	Type	Description
ARC_DBG_TF	O	Indicates that a triple fault exception has occurred
ARC_WDT_RESET	O	Watchdog reset
CLK24M_OUT	O	Output clock 48 MHz/2, in some USB purposes
CLK25M	I	PLL Reference Clock 25 MHz
GPIO8[7:0]	IO	SM GPIO Data
I2C0_SCL	IO	SM I²C clock
I2C0_SDA	IO	SM I²C data
RESET_N	I	System reset, active low
SMB0_CLK	IO	SM SMBus clock
SMB0_DAT	IO	SM SMBus data
SPI0_CLK	O	Output clock
SPI0_RXD	I	Receive data
SPI0_SS_N[3:0]	O	Slave select
SPI0_TXD	O	Transmit data
TEST_0	I	Test point 0. Connect to ground **NOTE:** Reserved in BE-M1000 manufactured since 2021.
TURBO_BOOT	I	Controls boot mode of the System Control Processor: 0 – 500 MHz (TURBO): 1 – 250 MHz. Connect through an external 10 kOhms resistor to 1.8 V
TRSTN	I	Test reset, active low
UART0_RXD	I	Receive data
UART0_TXD	O	Transmit data

5.1.6 System Debug

Table 5-21 system debug pins

Pin name	Type	Description
CS_CLK	O	Trace port clock
CS_CTRL	O	Trace port control
CS_DAT[15:0]	O	Trace port data
CS_SWCLK_TCK	I	Serial wire and TAP clock
CS_SWDIO_TMS	IO	Combined serial wire input/output
CS_TDI	I	JTAG TAP data IN
CS_TDO	O	JTAG TAP data OUT
CS_TRST_N	I	TAP Asynchronous reset, active low

5.1.7 Power and Ground

5.1.7.1 Core Supply

Table 5-22 core supply pins

Pin name	Type	Description
VDD	P	Core power supply

5.1.7.2 0.95V Voltage Supply

Table 5-23 0.95V voltage supply pins

Pin name	Type	Description
VDD_HDMI_09	P	0.9 V analog power supply
VDD_PCIE4_0_09	P	PCIE4_0 analog power supply
VDD_PCIE4_1_09	P	PCIE4_1 analog power supply
VDD_PCIE8_09	P	PCIE8 analog power supply
VDD_SATA_09	P	SATA analog and digital power supply
VDD_SATATX_09	P	SATATX power supply
VDD_USB2_09	P	USB2 digital power supply
VDD_USB3_0_09	P	USB3_1 analog and digital high-speed power supply
VDD_USB3_1_09	P	USB3_1 analog and digital high-speed power supply
VDD_USB3TX_0_09	P	USB3TX_0 transmit power supply
VDD_USB3TX_1_09	P	USB3TX_1 transmit power supply
VDD_USB3VP_0_09	P	USB3VP_0 analog and digital SuperSpeed power supply
VDD_USB3VP_1_09	P	USB3VP_1 analog and digital SuperSpeed power supply
VDD_XG0_09	P	XG0 analog power supply
VDD_XG1_09	P	XG1 analog power supply

5.1.7.3 PLL Supply

Table 5-24 PLL supply pins

Pin name	Type	Description
VDDPLL_0_09	P	PLL_0 power supply
VDDPLL_1_09	P	PLL_1 power supply
VDDPLL_2_09	P	PLL_2 power supply
VDDPLL_3_09	P	PLL_3 power supply
VDDPLL_HDMI_09	P	PLL_HDMI power supply

5.1.7.4 DDR Supply

Table 5-25 DDR supply pins

Pin name	Type	Description
VDDQ_DDR0	P	VDDQ_DDR0 power supply
VDDQ_DDR1	P	VDDQ_DDR1 power supply

5.1.7.5 1.5V Voltage Supply

Table 5-26 1.5V voltage supply pins

Pin name	Type	Description
VDD_PCIE4_0_15	P	PCIE4_0 IO power supply
VDD_PCIE4_1_15	P	PCIE4_1 IO power supply
VDD_PCIE8_15	P	PCIE8 IO power supply
VDD_XG0_15	P	XG0 IO power supply
VDD_XG1_15	P	XG1 IO power supply

5.1.7.6 1.8V Voltage Supply

Table 5-27 1.8V voltage supply pins

Pin name	Type	Description
VDD_DDR0_PLL	P	DDR0_PLL power supply
VDD_DDR1_PLL	P	DDR1_PLL power supply
VDD_HDMI_18	P	HDMI analog power supply
VDD_PVT_18	P	PVT sensor power supply
VDD_SATA_18	P	SATA PHY high-voltage power supply
VDD_USB2_18	P	USB2 analog power supply
VDDIO_18	P	IO power supply
VDD_FUSE_18	P	SM power supply **NOTE:** This signal is not used in normal operating mode and must be floating or tied to the ground.

5.1.7.7   3.3V Voltage Supply

Table 5-28 3.3V voltage supply pins

Pin name	Type	Description
VDD_SD_33	P	SD power supply
VDD_USB2_0_33	P	USB2_0 analog power supply
VDD_USB2_1_33	P	USB2_1 analog power supply
VDD_USB2_2_33	P	USB2_2 analog power supply
VDD_USB2_3_33	P	USB2_3 analog power supply
VDD_USB3_33	P	USB3 high power supply for HS operation & SS operation

5.1.7.8   Ground

Table 5-29 ground pins

Pin name	Type	Description
VSS	G	Core ground
VSSIO	G	IO ground
VSSPLL_0	G	PLL ground
VSSPLL_1	G	PLL ground
VSSPLL_2	G	PLL ground
VSSPLL_3	G	PLL ground
VSSPLL_HDMI	G	PLL_HDMI ground

5.1.8   Requirements for Unused Pins

The following table shows the requirements for unused pins of the BE-M1000. Please follow these requirements if you are not going to use any interface from **Pinout List**.

Table 5-30 Requirements for unused pins

Type	Requirements
Input pins	Tie to ground potential If active signal is low, tie to power supply
Output pins	Leave floating
Power pins	Always use
Reserved pins	Leave floating

5.2 Pin Map Overview

The diagrams below show pinout from the top view of the package.

Figure 5-1 BE-M1000 pin map

5.2.1 Power and Ground
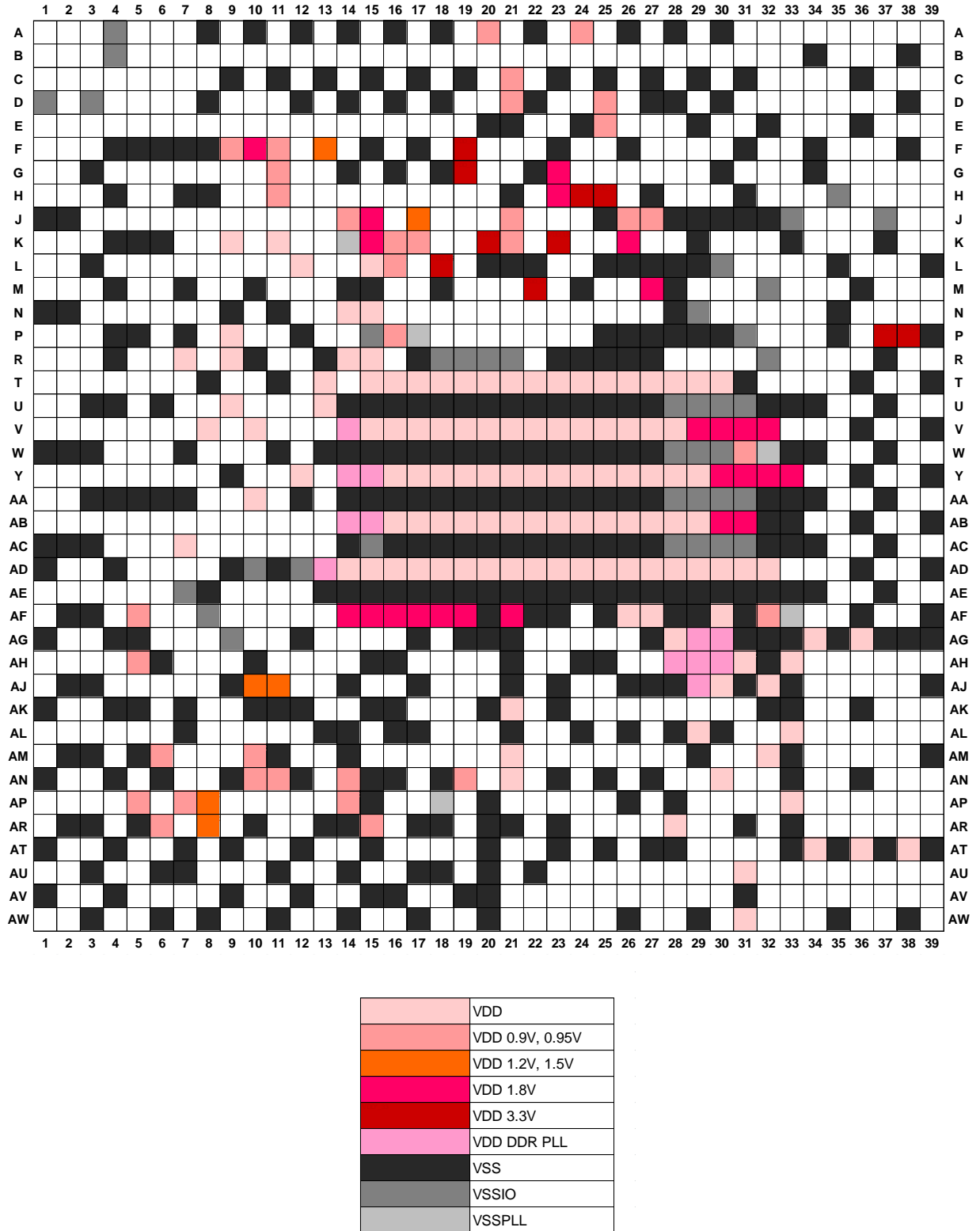
Figure 5-2 Power and ground pin placement

5.2.2 High Speed Peripherals
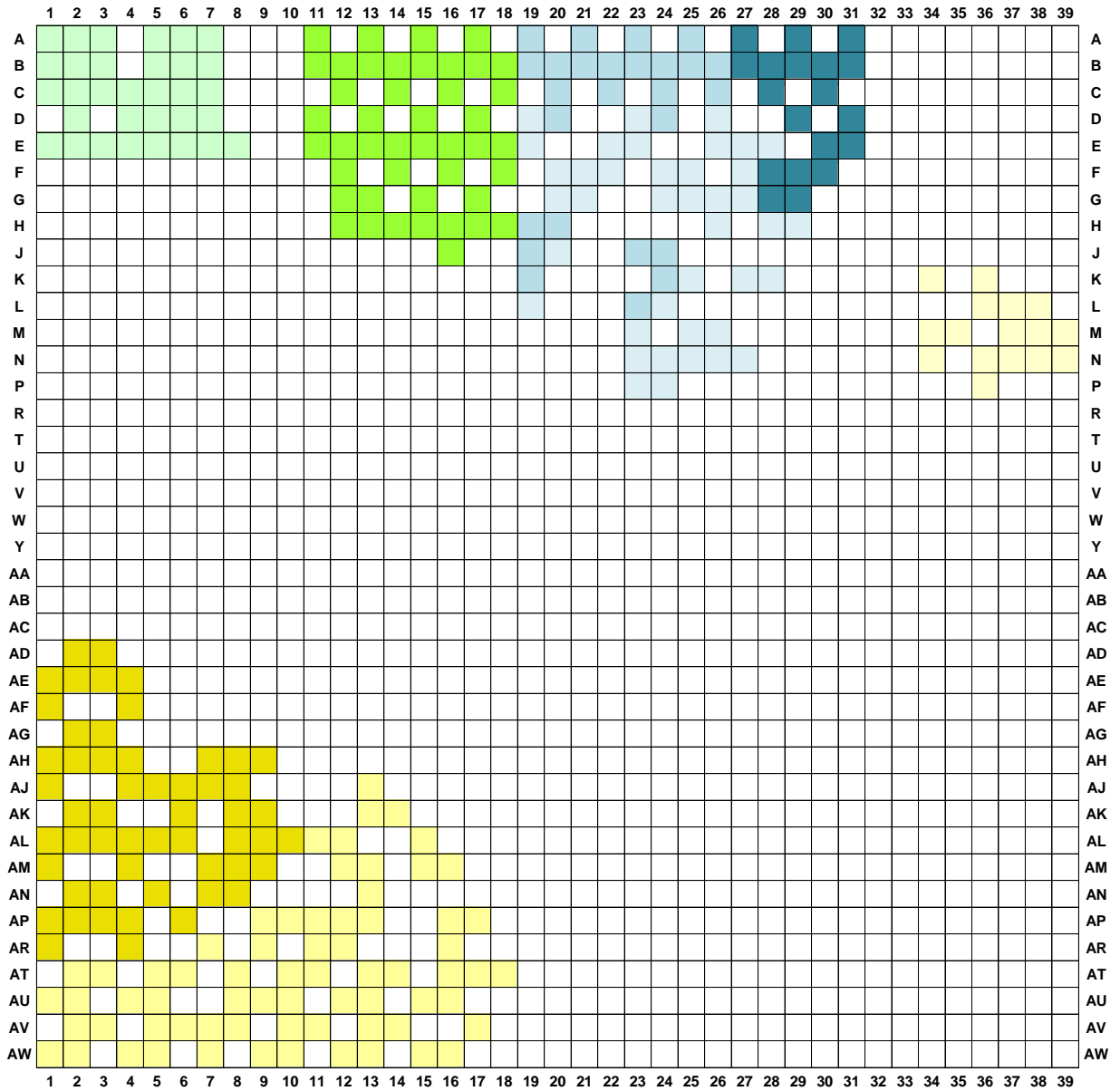
Figure 5-3 High speed peripherals pin placement

5.2.3 Low Speed Peripherals
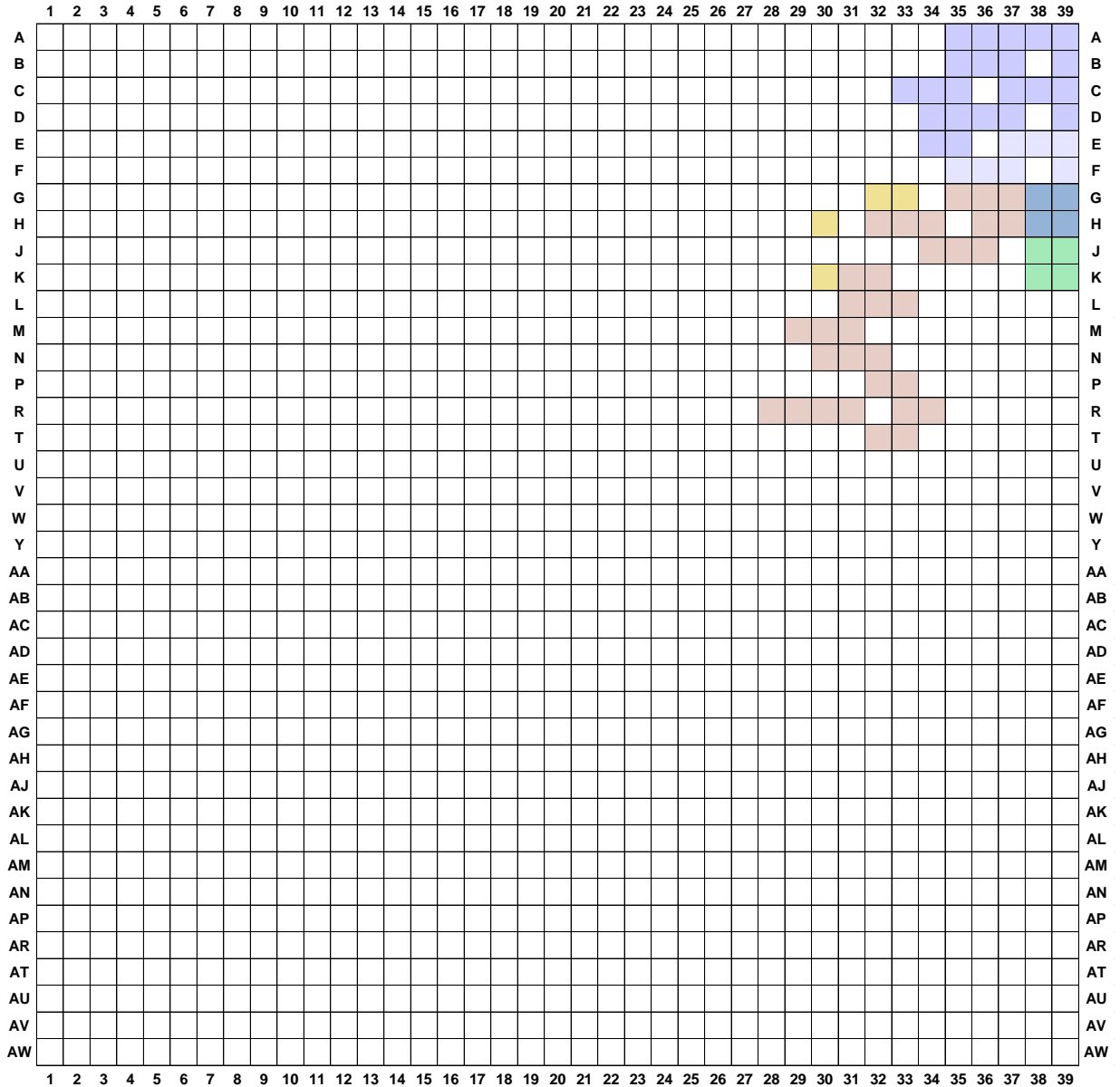
Figure 5-4 Low speed peripherals pin placement

5.2.4 Memory
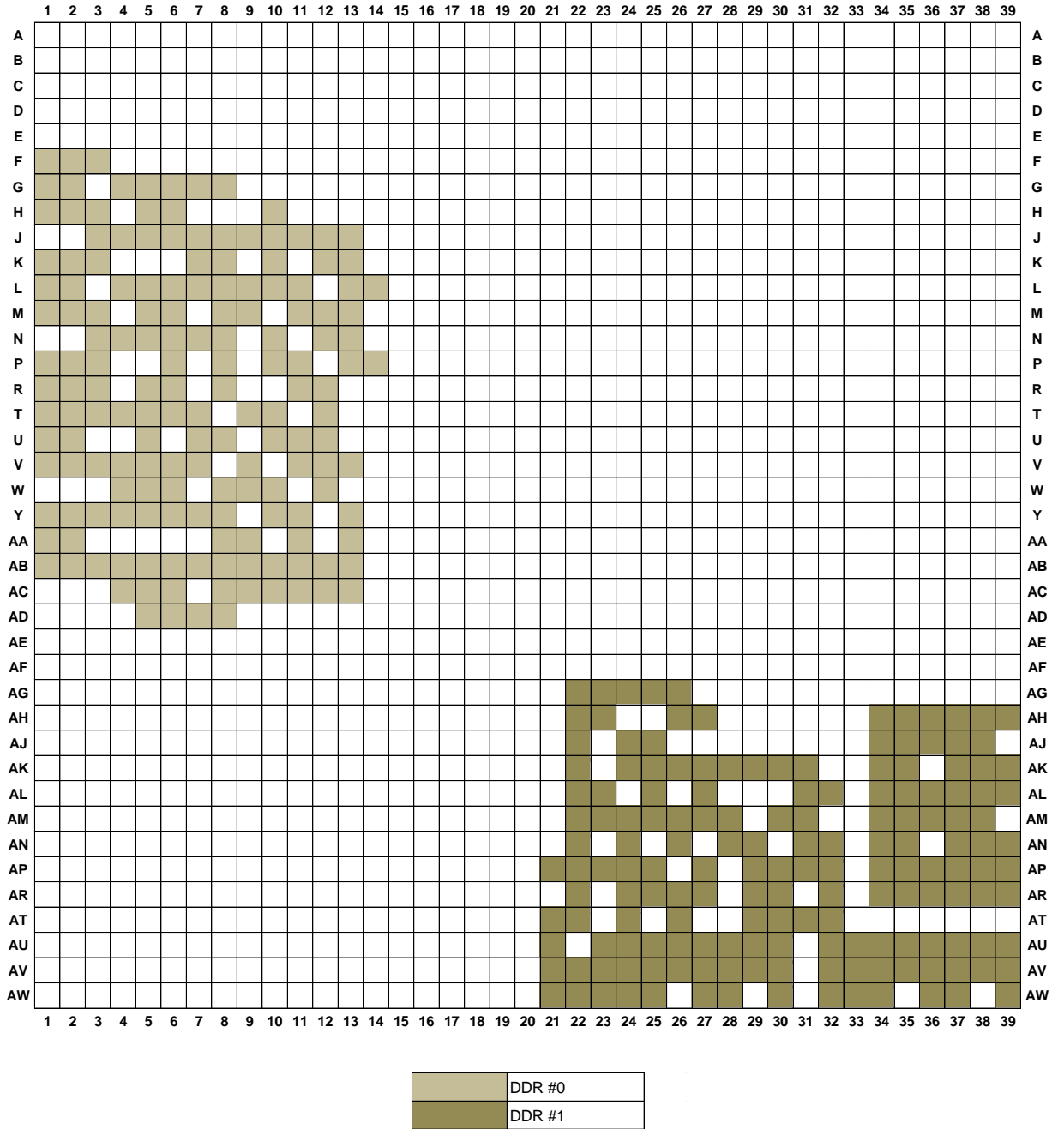
Figure 5-5 Memory pin placement

5.2.5 Audio and Video
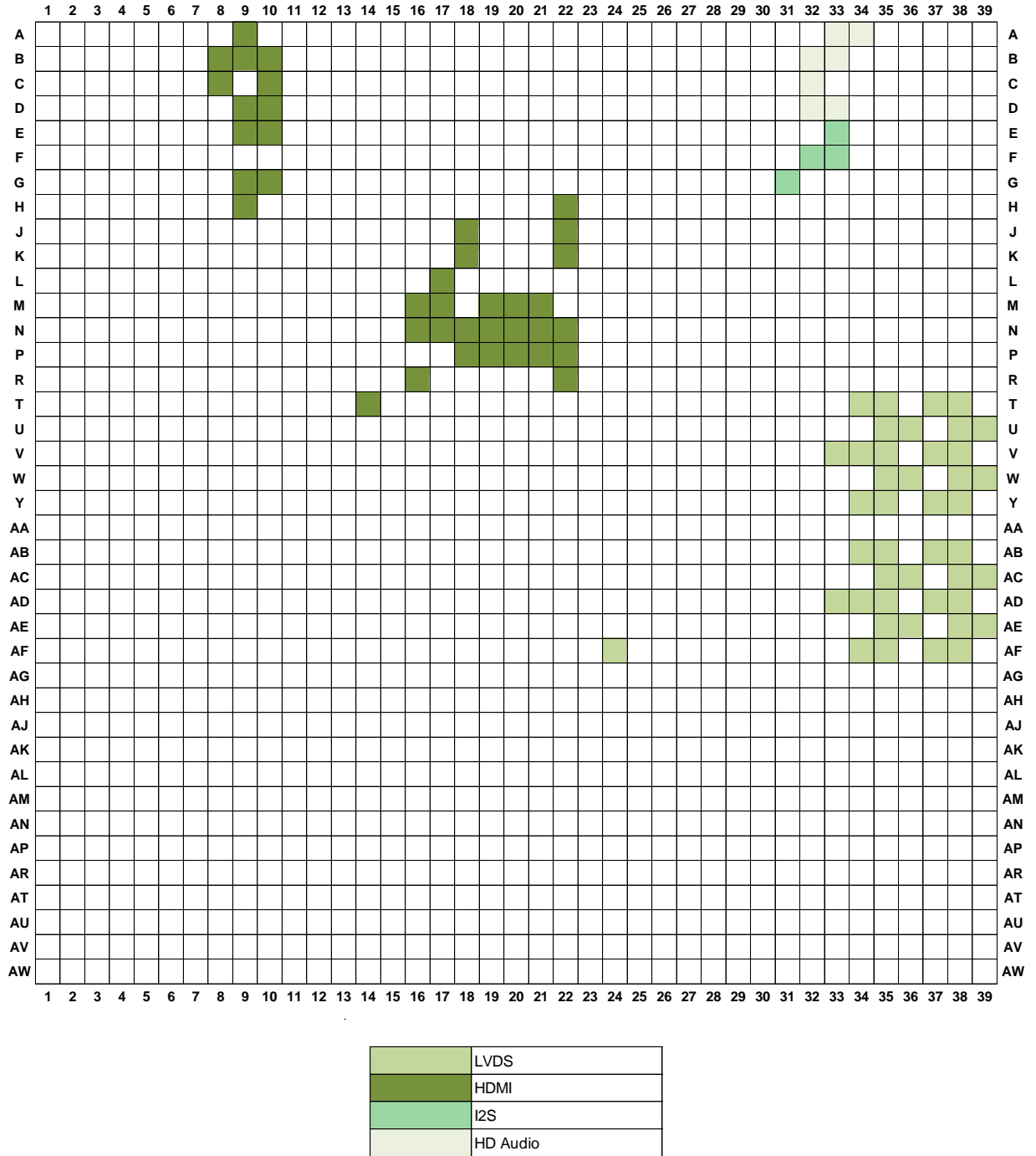
Figure 5-6 Audio and video pin placement

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5.2.6 System Control and Debug
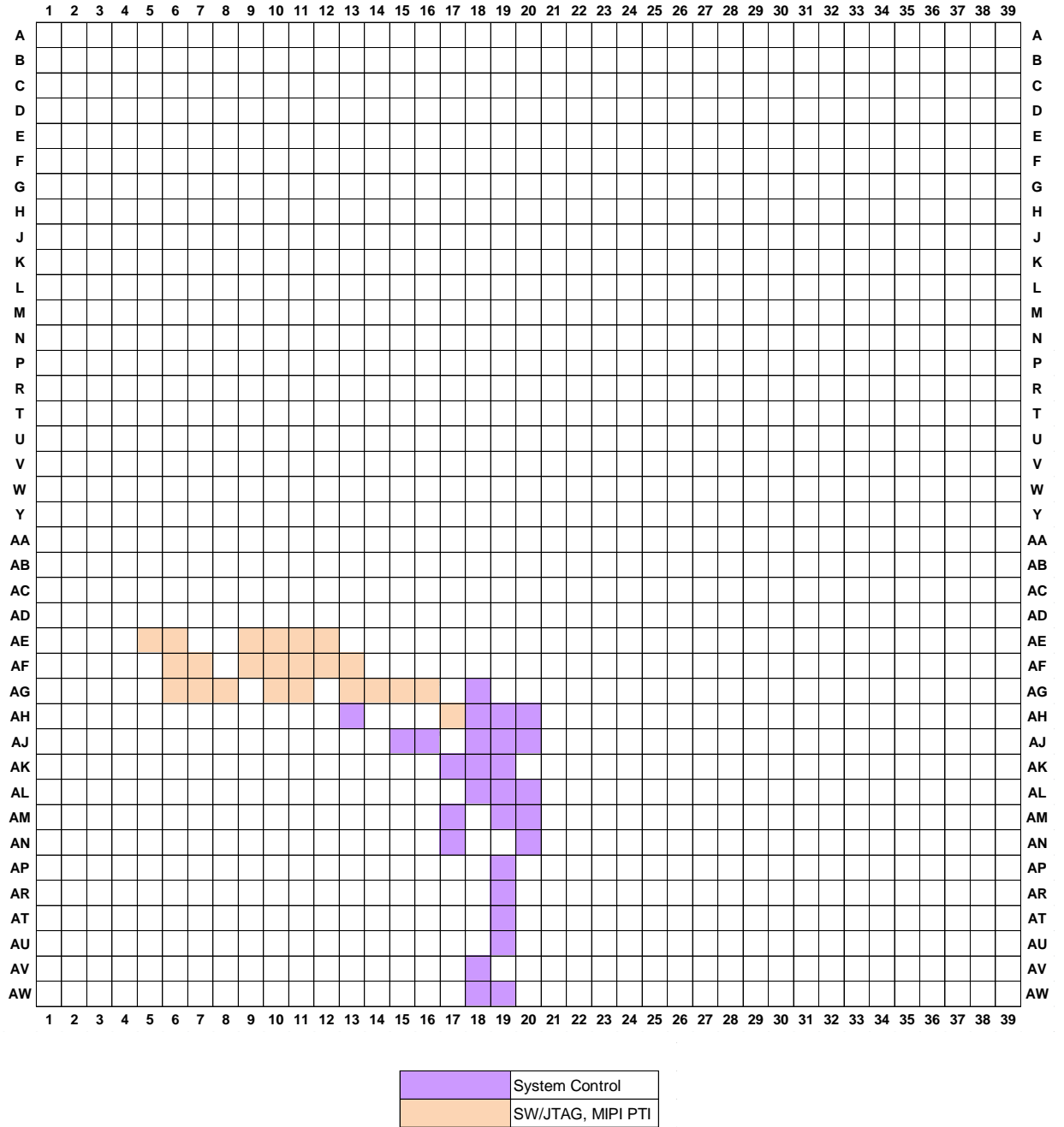
Figure 5-7 System control and debug pin placement

6 Package and Ordering Information

6.1 Ordering Information

BE-M1000 is an orderable part number. Designation of each field in the part number are shown in a table below.

Table 6-1 Ordering information

BE	-	M	1	0	0	0
Baikal Electronics	Field Delimiter	Product Line	Generation	Modification	Reserved Field	Reserved Field

BE-M1000 is the first product in BE-M product line.

To order BE-M1000, please contact BAIKAL ELECTRONICS company.

6.2 Marking

The following table describes the options of BE-M1000 marking.

Table 6-2 BE-M1000 package marking options

	Marking	Arm logo
1	WW.YYYY	ARM
2	WW.YYYY	arm
3	BA.YYWW	arm
4	BN.YYWW	arm
5	BK.YYWW	arm

The following table shows designation of each field in the package marking of BE-M1000 #1 and #2 packages.

Table 6-3 BE-M1000 #1 and #2 packages marking

WW	.	YYYY
Week	Field Delimiter	Year

The following table shows designation of each field in the package marking of BE-M1000 #3 to #5 packages.

Table 6-4 BE-M1000 #3 to #5 packages marking

XX	.	YY	WW
Package Type	Field Delimiter	Year	Week

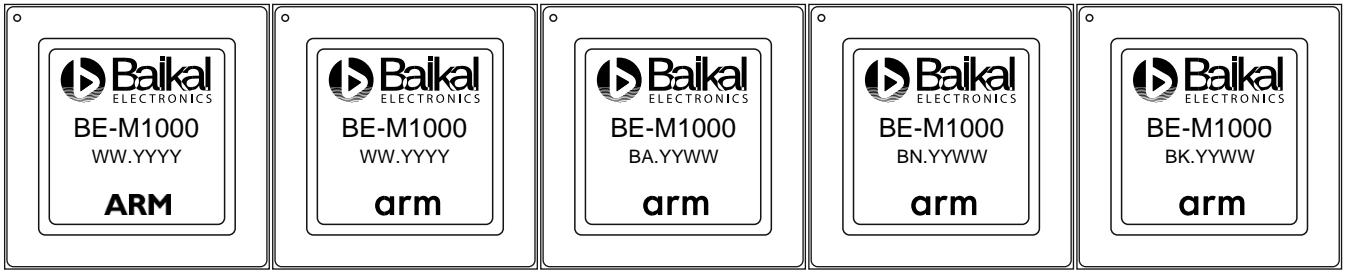The following figures show the top view of the BE-M1000 microprocessors in different packages.

Figure 6-1 BE-M1000. Top view

6.3   FCBGA-1521 Package

The SoC is mounted into FCBGA-1521 package. Main package parameters are shown it the figures and table below.
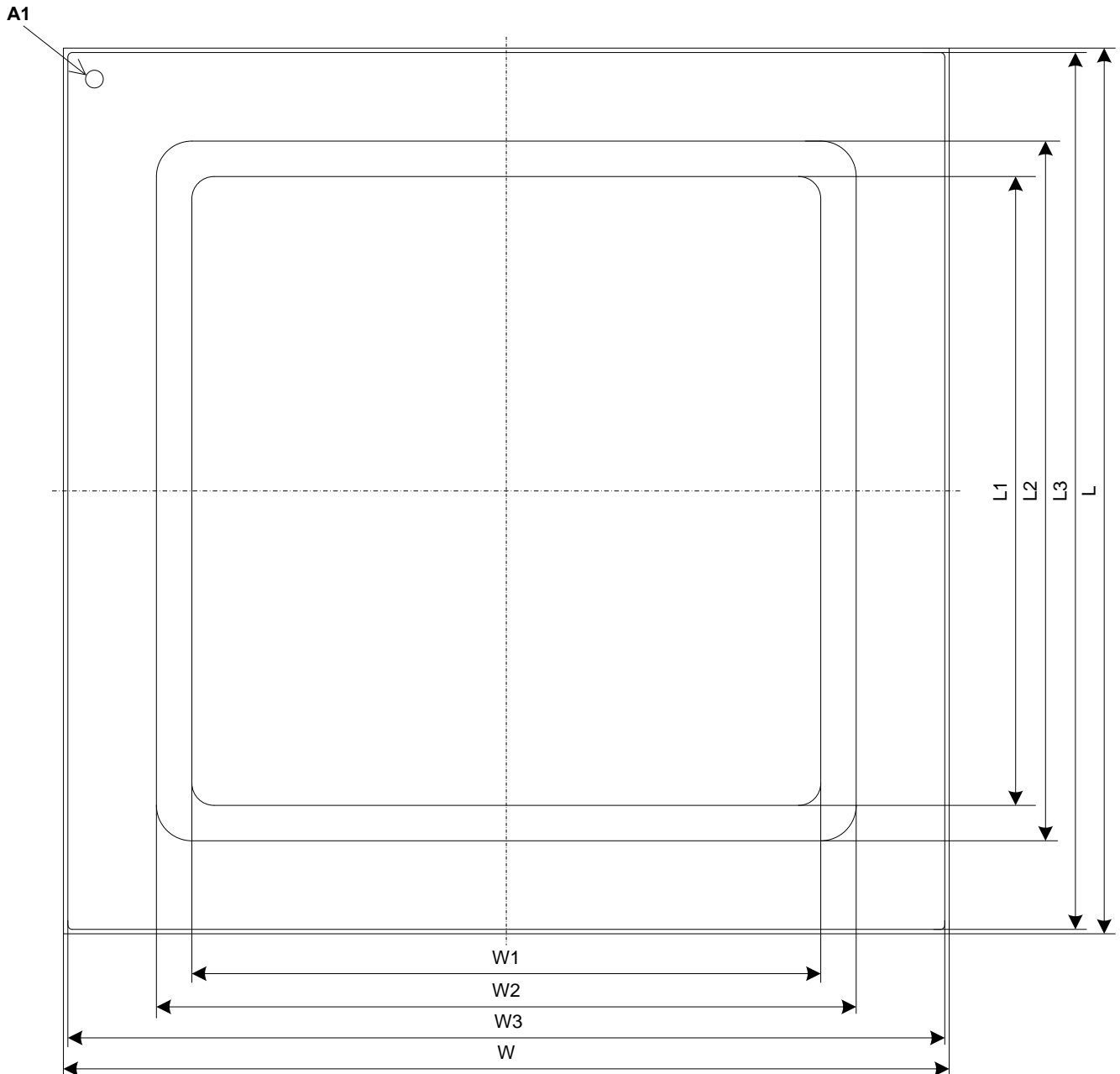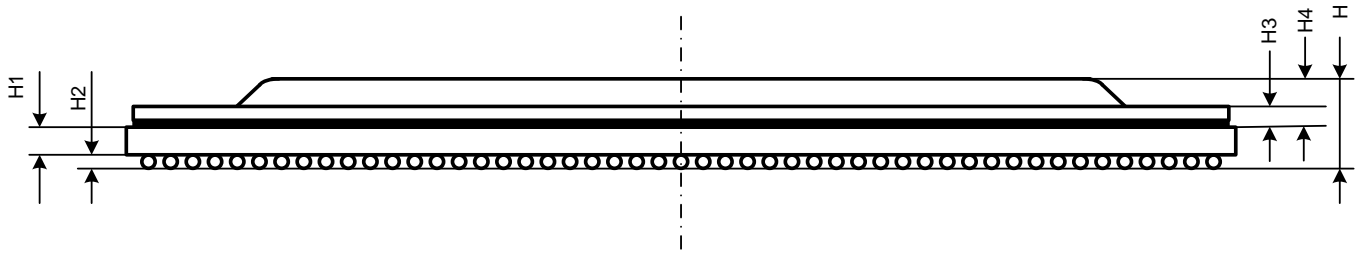

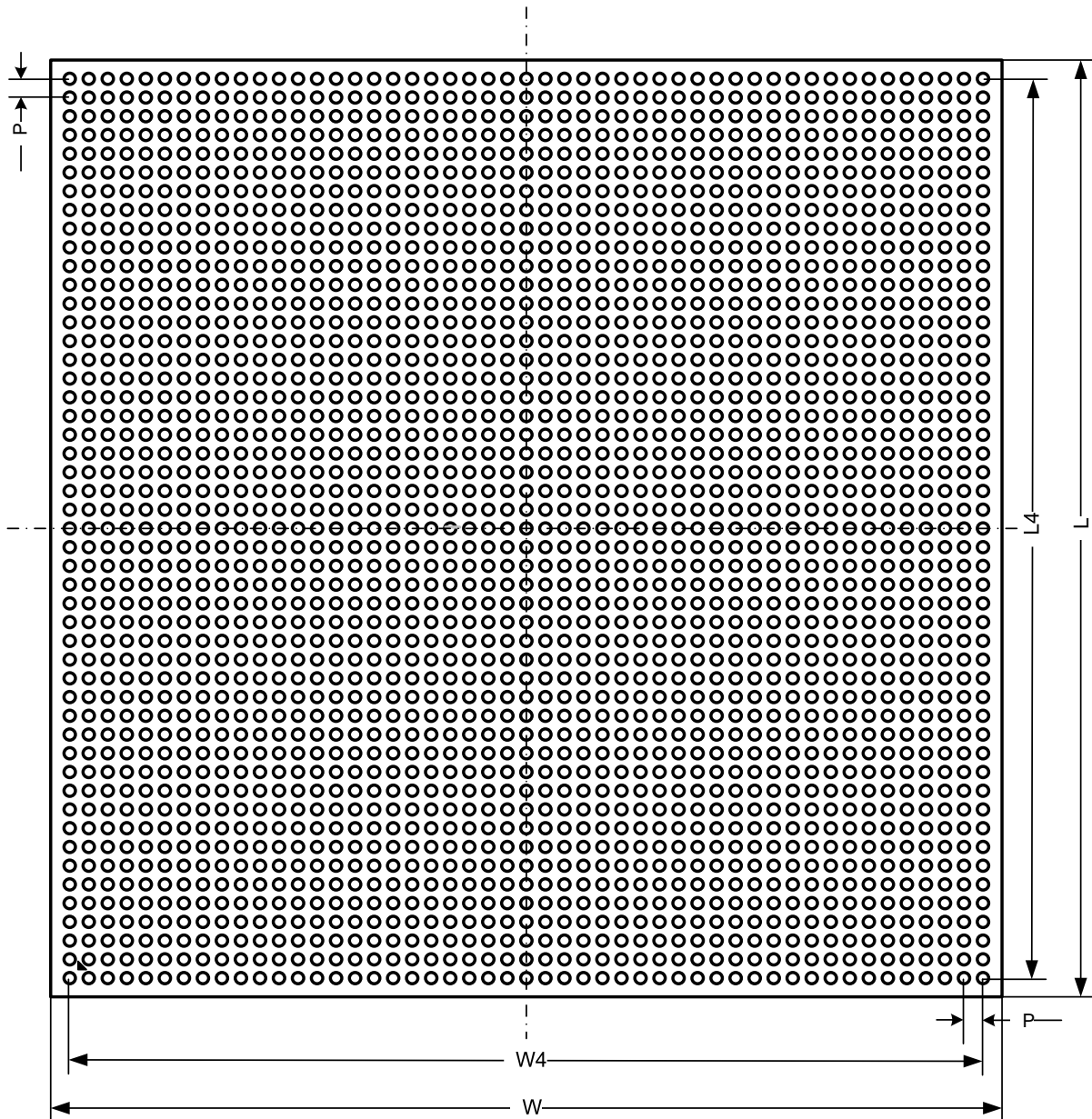**Figure 6-2 SoC package. Top view**

Figure 6-3 SoC package. Side view

Figure 6-4 SoC package. Bottom view

The following table shows the package parameters.

Table 6-5 Package parameters

Symbol	Value, mm	Description
L	40,00	Package length
L1	28,40	Upper cover part length
L2	31,60	Bottom cover part length
L3	39,60	Cover length
L4	38,00	Edge ball center to center
W	40,00	Package width
W1	28,40	Upper cover part width
W2	31,60	Bottom cover part width
W3	39,60	Cover width
W4	38,00	Edge ball center to center
H	2,676…3,176	Package thickness including balls
H1	1,026	Substrate thickness
H2	0,40	Ball height
H3	0,50	Heat sink cover thickness
H4	1,30	Heat sink cover height
D	0,60	Ball diameter
P	1,00	Ball pitch

6.4 Packing

The BE-M1000 microprocessors are shipped in trays, 21 pieces per tray. A package may contain not more than 30 trays. The unused space is filled with a soft sealing materialIlf less than 30 trays are stacked in the package. The space between trays is padded with a soft sealing material. The following figure shows a sketch diagram of the package.
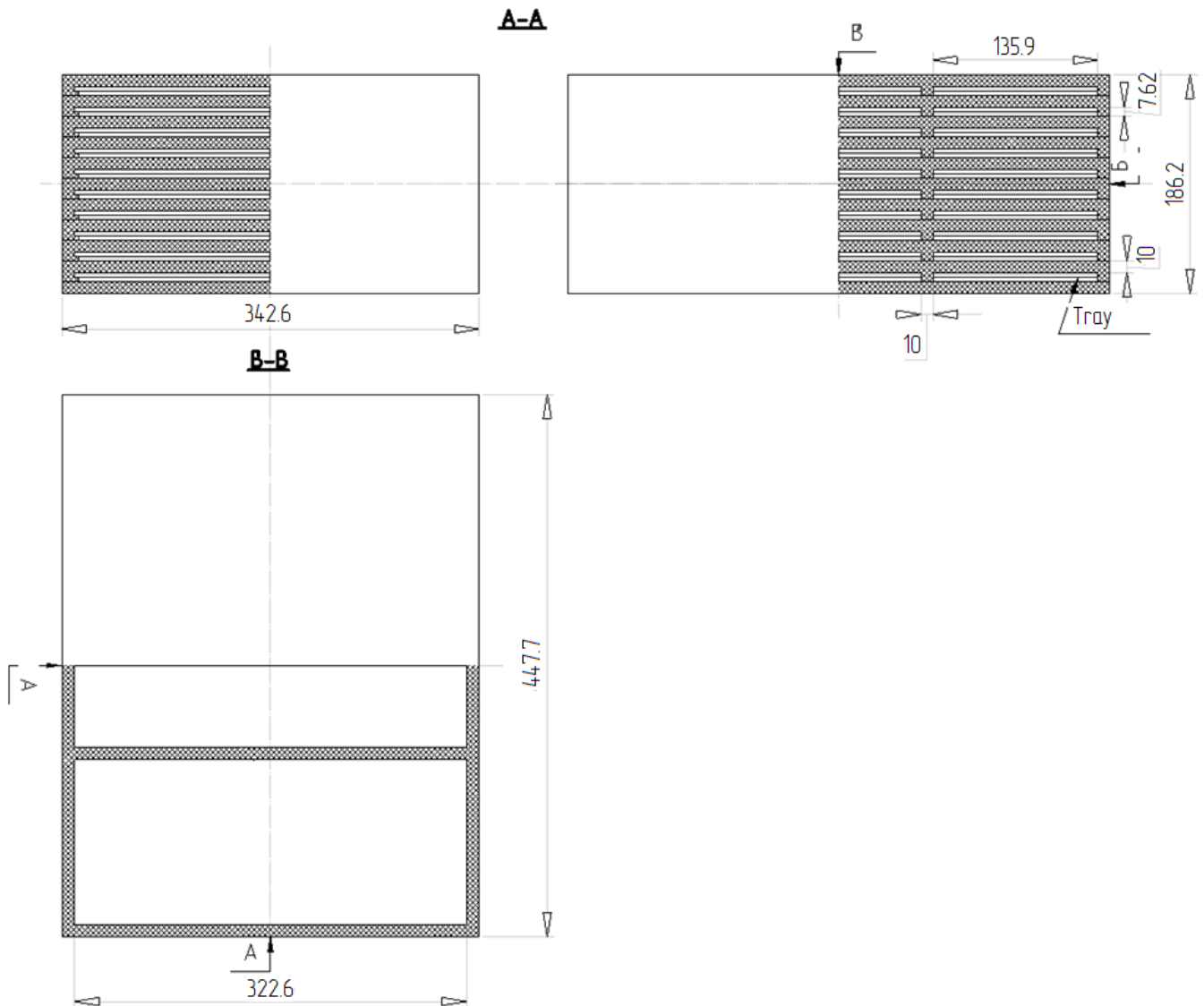

Figure 6-5 BE-M1000 packing tray overview

6.5 Soldering

For different batches of microprocessors, the appropriate requirements for the soldering process must be applied. The soldering method choice depends on the type of the microprocessor batch Marking:

- Soldering for packages marked BN
- Soldering for packages marked BA or BK

6.5.1 Soldering for packages marked BN

Before soldering, solder paste must be applied to the contact pads of the *Printed Circuit Board* (**PCB**). It's recommended to use pastes with 62Sn/36Pb/2Ag composition.

Corresponding modes and temperatures are described in the following table and figure.

Table 6-6 Temperature profile for SoC soldering to PCB (BN)

Profile feature	Description	Temperature	Duration
A	Ramp-up rate	3°C/sec max.	
B	Preheat stage	78…162°C	~140 seconds
C	Ramp-up rate	3°C/sec max.	
D	Melting stage	>190°C	~80 seconds
E	Soldering stage	>208°C	30-40 seconds
F	Peak temperature	215°C	
G	Time from room temperature to peak temperature		306.3 seconds
H	Ramp-down rate	1°C/sec max.	

WARNING: When adjusting the soldering profile for a specific PCB instance, it's strongly recommended not to exceed 215 °C.
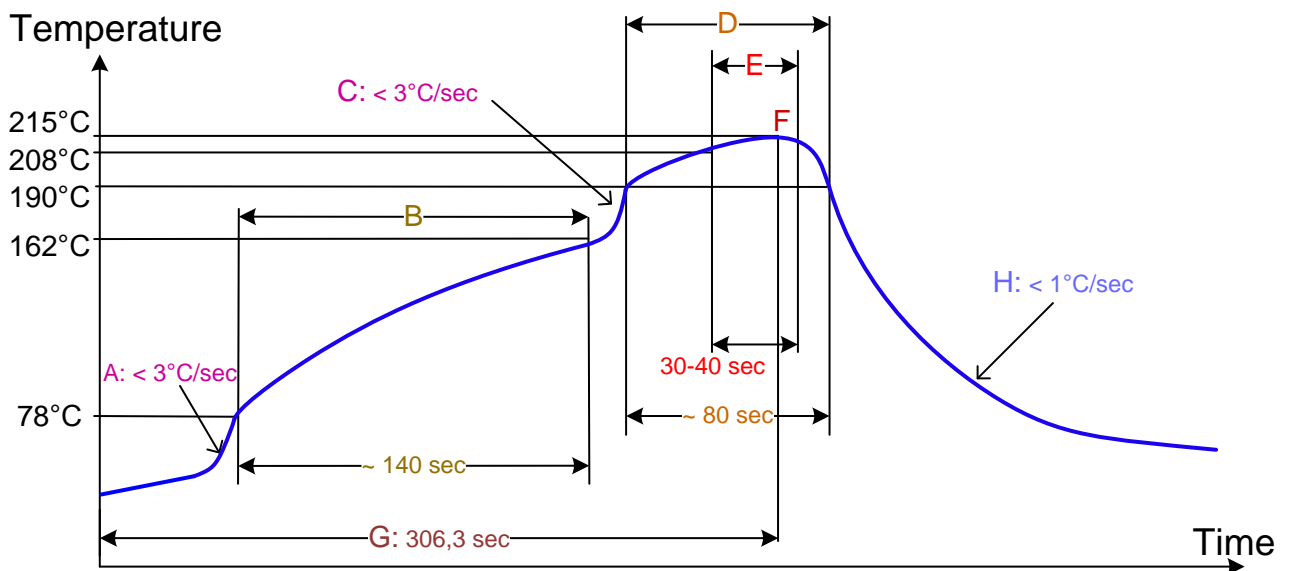

Figure 6-6 Soldering profile for packages marked BN

6.5.2 Soldering for packages marked BA or BK

SoC mounting to PCB should be accomplished in accordance with the soldering profile recommended for Pb-Free packages.

Corresponding modes and temperatures are described in the following table and figure.

Table 6-7 Temperature profile for SoC soldering to PCB (BA or BK)

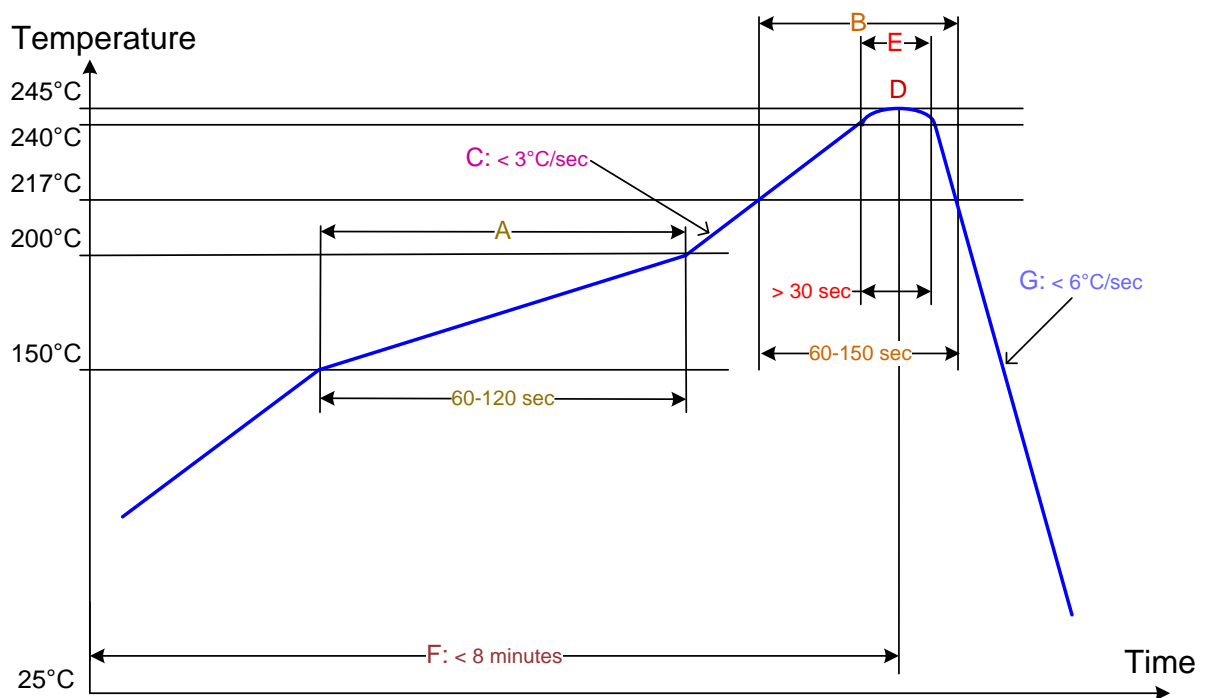| Profile feature	Description	Temperature	Duration
A	Preheat stage	150…200°C	60…120 seconds
B	Melting stage	>217°C	60…150 seconds
C	Ramp-up rate	3°C/sec max.	
D	Peak temperature	245°C	
E	Soldering stage	>240°C	30 seconds min.
F	Time from room temperature to peak temperature		< 8 minutes max.
G	Ramp-down rate	6°C/sec max.	

Figure 6-7 Soldering profile for packages marked BA or BK

7 Support

7.1   Documentation

The following documents describe the BE-M1000 microprocessor and provide information for board designers and system programmers:

- Application Design Guide

- Thermo-Mechanical Design Guide

- Programming Guide

- Power Supply Requirements

7.1.1 Application Design Guide

The *Application Design Guide* (**ADG**) describes how to design the BE-M1000 physical interfaces on a board.

ADG is available in English only. To request the guide, please contact BAIKAL ELECTRONICS support. **NDA is required**.

The following table describes the guide content.

Table 7-1 BE-M1000 application design guide

Volume	Title
1	DDR3/4
2	PCIe
3	USB 3.0 and USB 2.0
4	10 Gb Ethernet
5	1 Gb Ethernet
6	SATA
7	eMMC/SD
8	SPI
9	eSPI
10	LVDS
11	HDMI
12	I^{2}S
13	MIPI PTI and SW/JTAG
14	High Definition Audio (HD Audio) Controller

7.1.2 Thermo-Mechanical Design Guide

The *Thermo-Mechanical Design Guide* (**TMDG**) is intended to assist board and system thermal mechanical designers, as well as designers and suppliers of processor heatsinks.

TMDG is released and available in Russian only (under the title «Руководство по термомеханическому проектированию»).

7.1.3 Programming Guide

The *Programming Guide* (**PG**) describes how to program the microprocessor subsystems and provides information for developers of device drivers or bare-metal applications.

PG is released and available in English only. To request the guide, please contact BAIKAL ELECTRONICS support. **NDA is required**.

The following table describes the guide content.

Table 7-2 BE-M1000 programming guide

	Volume	Title
1	1	General Description
2	2	Memory Map
3	3	Interrupts
		SoC Interconnects
4	4.1	Network Interconnect (NIC)
5	4.2	Cache Coherent Network (CCN)
		System Debug
	5	CoreSight Subsystem
		System Monitoring and Management
7	6.1	Local Clock and Reset Unit (LCRU)
8	6.2	Process, Voltage and Temperature (PVT) Sensors
		Memory Management
9	7.1	DDR3/4 Memory Controller
10	7.2	DDR PHY
11	7.3	System Memory Management Unit (SMMU)
12	7.4	DMA Controller for Low Speed Peripherals (DMA LSP)
13	7.5	DMA Controller for Mem2Mem Transfers
		Connectivity & Mass Storage
14	8.1	USB 2.0 Controller
15	8.2	USB 3.0/2.0 Controller
16	8.3	PCI Express (PCIe)
17	8.4	1Gb Ethernet MAC (GMAC)
18	8.5	10Gb Ethernet MAC (XGMAC)
19	8.6	PCIe & XGMAC PHY
20	8.7	Serial ATA 6G (SATA)
21	8.8	Mobile Storage Host Controller (eMMC/SD)
22	8.9	USB 3.0/2.0 PHY
23	8.10	SATA PHY
		Timers
24	9.1	Cortex-A57 Timers
25	9.2	Peripheral Timers
		Multimedia and Graphics
26	10.1	Mali Graphics Processing Unit (Mali GPU)
27	10.2	HDMI Controller
28	10.3	HDMI PHY
29	10.4	Video Display Unit (VDU) for HDMI and LVDS
30	10.5	HD Video Decoder
31	10.6	Inter-IC Sound Bus (I2S)
32	10.7	HD Audio Controller
		Low Speed Communication and Interconnects
33	11.1	Inter-IC Controller (I2C)
34	11.2	Serial Peripheral Interface (SPI)
35	11.3	Enhanced Serial Peripheral Interface (eSPI)
36	11.4	Universal Asynchronous Receiver/Transmitter (UART)
37	11.5	System Management Bus Controller (SMBus)
38	11.6	General Purpose Input/Output (GPIO)
		Security
39	12.1	TrustZone Management
40	12.2	TrustZone Controller

7.1.4 Power Supply Requirements

Each power domain of BE-M1000 requires the use of special filters on the power supply. The power supply requirements are describes in the document written in Russia under the title «Микропроцессор BE-M1000 Требования к источникам питания».

7.2   SDK

BAIKAL ELECTRONICS produces the *Software Development Kit* (**SDK**) ARM64, which provides software support for the BE-M1000 microprocessor.

To provide your application compatibility with the SDK ARM64, you should follow the requirements described in the document written in Russian under the title «Базовый набор требований и рекомендаций по построению аппаратных платформ на базе СнК (SoC) BE-M1000».
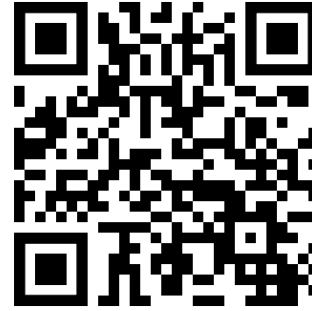
For details on the SDK ARM64, refer to the document under the title:

- «Обзор Baikal ARM64 SDK» (written in Russian)

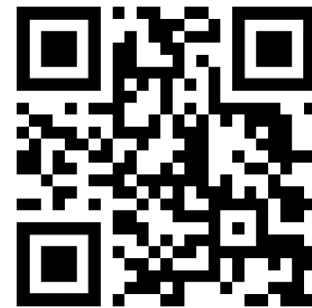- «Baikal ARM64 SDK Overview» (written in English)

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Revision History

Revision	Date	Substantive change(s)
0.65	02.07.2019	Initial version
0.70	01.11.2019	Updated 4 Power-Up/Down
0.73	16.12.2019	In 5.1 Pinout List, changed the following pin IDs: DDR0_DQ[18], DDR0_DQ[19], DDR0_DQ[20], DDR0_DQ[21], DDR0_DQ[26], DDR0_DQ[27], DDR0_DQ[28], DDR0_DQ[29], DDR0_DQ[41], DDR0_DQ[44], DDR0_DQ[48], DDR0_DQ[51], DDR0_DQ[52], DDR0_DQ[53], DDR0_DQ[56], DDR0_DQ[63]
0.74	04.03.2020	Updated 2.4 System Control Module
0.82	25.05.2020	Updated 4.1 Power-Up Sequence
0.83	13.07.2020	For Arm Mali-T628 GPU, the operating frequency of shader cores changed from **500 MHz** to **700 MHz**
0.84	22.10.2020	• For Arm Mali-T628 GPU, the operating frequency of shader cores changed from **700 MHz** to **750 MHz** • **4K Video Decoder** has been renamed to **HD Video Decoder** due to limited support for 4K@30fps video formats • **LVDS:** max display resolution changed to **up to 2560x1440** • **HDMI:** max display resolution changed to **up to 3840x2160** • Updated 3.1 Power Supply Parameters • Added 5.1.1 Requirements for Unused Pins
0.85	11.11.2020	In 5.1.4.1 LVDS, pins LVDS_L*_DATN[4] and LVDS_L*_DATP[4] moved to N/C group and marked as Reserved because VDU does not use Channel 4 for supported data formats
0.88	04.06.2021	In 2.4.7 VDU with HDMI 2.0, max display resolution changed from **3840x2160** to **2560x1440**
0.89	15.06.2021	Updated 3 Electrical Specifications
0.91	28.06.2021	Updated 1.1 Main Features
0.92	14.07.2021	In section 5.1.5 System Control, changed **Pin Name** and **Description** for the TURBO_BOOT (AL18) pin
0.94	11.10.2021	Added: • 2.7.5 HD Audio • 5.1.4.3 HD Audio • 6.1 Marking In 5.1 Pinout List tables, the **Pin Description** column is added with information about differences in packages
0.953	13.01.2022	Updated 6.1 Marking
0.954	17.02.2022	In 4.1 Power-Up Sequence, added the start sequence diagram

Revision	Date	Substantive change(s)
0.956	28.04.2022	Added: • 6.4 Packing • 7.1.1 Power Supply Requirements • 7.2 SDK
1.00	04.07.2022	Released
1.01	01.08.2022	Updated 4 Power-Up/Down
1.05	08.09.2022	Updated 6.5 Soldering
1.10	16.02.2023	Minor edits